



SPEChpc™ 2021 Small Result

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Transtec

(Test Sponsor: Helmholtz-Zentrum Dresden - Rossendorf)

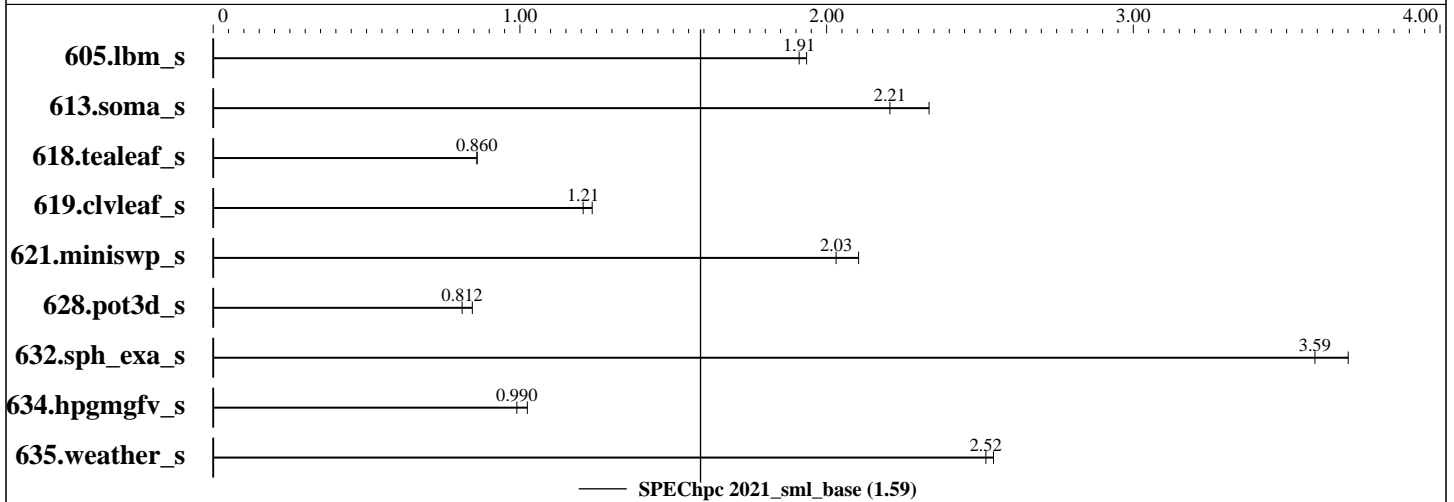
SPEChpc 2021_sml_base = 1.59

SPEChpc 2021_sml_peak = Not Run

Hemera: Intel Server Board S2600BPB (Intel Xeon Gold 6148)

hpc2021 License: 065A
Test Sponsor: Helmholtz-Zentrum Dresden - Rossendorf
Tested by: Helmholtz-Zentrum Dresden - Rossendorf

Test Date: Sep-2021
Hardware Availability: Jul-2017
Software Availability: Oct-2020



Results Table

Benchmark	Base								Peak										
	Model	Ranks	Thrds/Rnk	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Model	Ranks	Thrds/Rnk	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	
605.lbm_s	OMP	16	20	801	1.93	811	1.91												
613.soma_s	OMP	16	20	725	2.21	685	2.33												
618.tealeaf_s	OMP	16	20	2385	0.860	2382	0.861												
619.clvleaf_s	OMP	16	20	1368	1.21	1335	1.24												
621.miniswp_s	OMP	16	20	542	2.03	523	2.10												
628.pot3d_s	OMP	16	20	2063	0.812	1983	0.845												
632.sph_exa_s	OMP	16	20	640	3.59	621	3.70												
634.hpgmgfv_s	OMP	16	20	985	0.990	952	1.02												
635.weather_s	OMP	16	20	1032	2.52	1022	2.54												

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.



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Hardware Summary

Type of System: Homogenous Cluster
Compute Node: Compute Node
Interconnect: Infiniband (EDR)
Compute Nodes Used: 8
Total Chips: 16
Total Cores: 320
Total Threads: 640
Total Memory: 3 TB
Max. Peak Threads: --

Software Summary

Compiler: Intel Parallel Studio XE 2020
MPI Library: --
Other MPI Info: --
Other Software: None
Base Parallel Model: OMP
Base Ranks Run: 16
Base Threads Run: 20
Peak Parallel Models: Not Run
Minimum Peak Ranks: --
Maximum Peak Ranks: --
Max. Peak Threads: --
Min. Peak Threads: --

Node Description: Compute Node

Hardware

Number of nodes: 8
Uses of the node: compute
Vendor: Intel
Model: Intel Server Board S2600BPB
CPU Name: Intel Xeon Gold 6148
CPU(s) orderable: 1 or 2 per node
Chips enabled: 2
Cores enabled: 40
Cores per chip: 20
Threads per core: 2
CPU Characteristics: Intel Turbo Boost Technology up to 3.7 GHz
CPU MHz: 2400
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core
L3 Cache: 28160 KB I+D on chip per chip
Other Cache: None
Memory: 384 GB (12 x 32GB 2Rx4 PC4-2666V-RB2-12)
Disk Subsystem: 1 x 500 GB SSD
Other Hardware: None
Accel Count: 0
Accel Model: --
Accel Vendor: --
Accel Type: --
Accel Connection: --
Accel ECC enabled: --
Accel Description: --
Adapter: Mellanox MT4115
Number of Adapters: 2
Slot Type: PCI-Express 3.0 x16
Data Rate: 100 Gb/s
Ports Used: 2
Interconnect Type: EDR Infiniband

Software

Accelerator Driver: --
Adapter: Mellanox MT4115
Adapter Driver: --
Adapter Firmware: 12.28.2006
Operating System: CentOS Linux release 7.9.2009 (Core)
3.10.0-1160.6.1.el7.x86_64
Local File System: xfs
Shared File System: GPFS Version 5.0.5.0
6 NSD (vendor: NEC)
5 building blocks (vendor: NetApp):
2x (240 x 8 TB HDD)
1x (180 x 12 TB HDD)
1x (240 x 16 TB HDD)
1x (120 x 16 TB HDD)
System State: Multi-user, run level 3
Other Software: None



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Interconnect Description: Infiniband (EDR)

Hardware

Software

Vendor: Mellanox Technologies
 Model: Mellanox SB7790
 Switch Model: 36 x EDR 100 Gb/s
 Number of Switches: 2
 Number of Ports: 36
 Data Rate: 100 Gb/s
 Firmware: --
 Topology: Mesh (blocking factor: 8:1)
 Primary Use: MPI Traffic, GPFS

: --

Submit Notes

The config file option 'submit' was used.

MPI startup command:

```
mpiexec.hydra --bind-to socket -np $ranks $command
```

General Notes

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC HPG Policy document, <http://www.spec.org/hpg/policy.html>

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Compiler Version Notes

```
=====
CC 605.lbm_s(base) 613.soma_s(base) 618.tealeaf_s(base) 621.miniswp_s(base)
   634.hpgmgfv_s(base)
-----
```

icc (ICC) 19.1.3.304 20200925

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Compiler Version Notes (Continued)

=====
CXXC 632.sph_exa_s(base)

icpc (ICC) 19.1.3.304 20200925
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
FC 619.clvleaf_s(base) 628.pot3d_s(base) 635.weather_s(base)

ifort (IFORT) 19.1.3.304 20200925
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

mpiicc

C++ benchmarks:

mpiicpc

Fortran benchmarks:

mpiifort

Base Portability Flags

605.lbm_s: -DSPEC_LP64
613.soma_s: -DSPEC_LP64 -DSPEC_NO_VAR_ARRAY_REDUCE
618.tealeaf_s: -DSPEC_LP64
619.clvleaf_s: -DSPEC_LP64
621.miniswp_s: -DSPEC_LP64
628.pot3d_s: -DSPEC_LP64
632.sph_exa_s: -DSPEC_LP64
634.hpgmgfv_s: -DSPEC_LP64
635.weather_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-Ofast -xCORE-AVX512 -qopenmp -ansi-alias

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Base Optimization Flags (Continued)

C++ benchmarks:

-Ofast -xCORE-AVX512 -qopenmp -ansi-alias

Fortran benchmarks:

-Ofast -xCORE-AVX512 -qopenmp

The flags file that was used to format this result can be browsed at

http://www.spec.org/hpc2021/flags/EM64T_Intel_flags.html

You can also download the XML flags source by saving the following link:

http://www.spec.org/hpc2021/flags/EM64T_Intel_flags.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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