SPEC CPU®2017 Integer Speed Result

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Hewlett Packard Enterprise

(Test Sponsor: HPE)
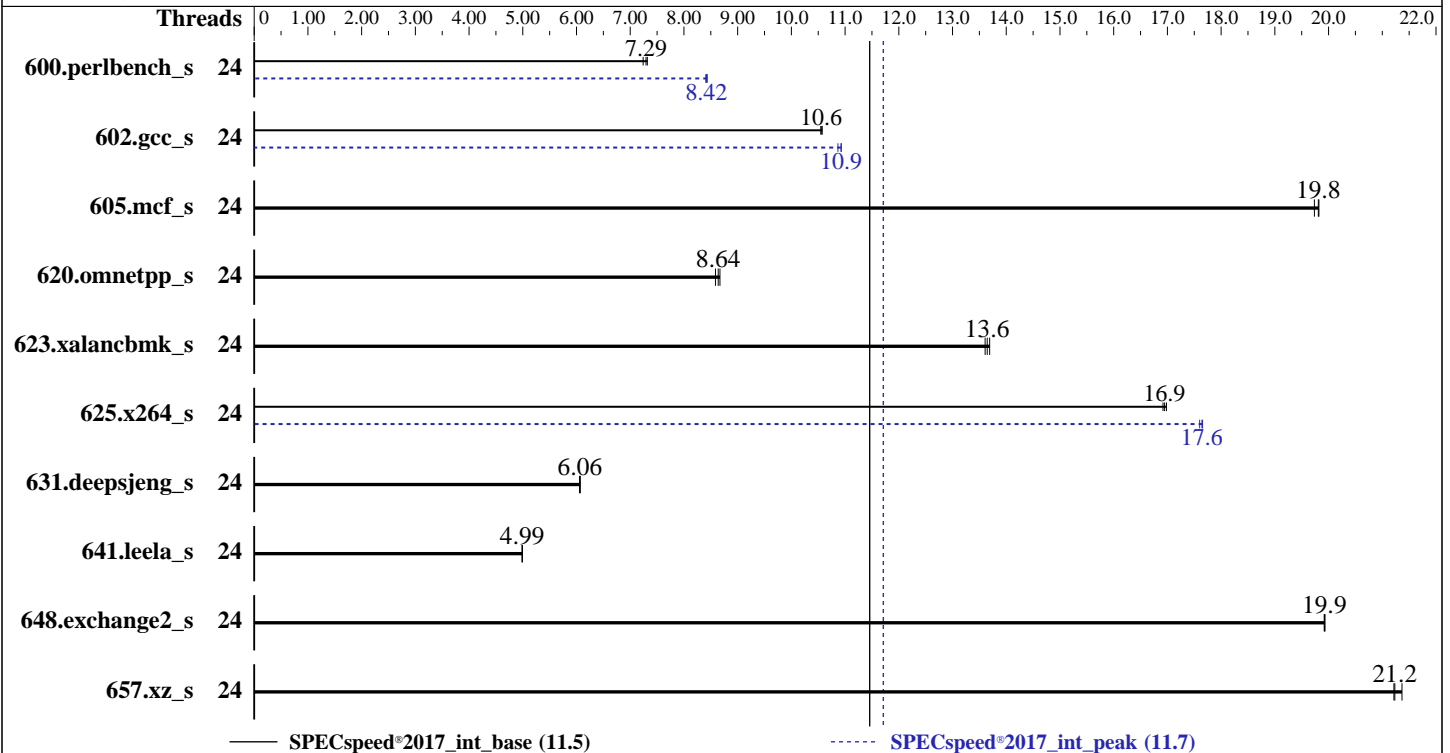
Synergy 480 Gen10 Plus
(3.00 GHz, Intel Xeon Gold 5317)

$SPECspeed®2017\_int\_base = 11.5$

$SPECspeed®2017\_int\_peak = 11.7$

CPU2017 License: 3

Test Sponsor: HPE

Tested by: HPE

Test Date: Dec-2021

Hardware Availability: Nov-2021

Software Availability: Dec-2020

Threads	0 1.00 2.00 3.00 4.00 5.00 6.00 7.00 8.00 9.00 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0 22.0
600.perlbench_s 24	7.29 / 8.42
602.gcc_s 24	10.6 / 10.9
605.mcf_s 24	19.8
620.omnetpp_s 24	8.64
623.xalancbmk_s 24	13.6
625.x264_s 24	16.9 / 17.6
631.deepsjeng_s 24	6.06
641.leela_s 24	4.99
648.exchange2_s 24	19.9
657.xz_s 24	21.2

——— SPECspeed®2017_int_base (11.5) ----- SPECspeed®2017_int_peak (11.7)

Hardware

CPU Name: Intel Xeon Gold 5317

 Max MHz: 3600

 Nominal: 3000

Enabled: 24 cores, 2 chips

Orderable: 1, 2 chip(s)

Cache L1: 32 KB I + 48 KB D on chip per core

 L2: 1.25 MB I+D on chip per core

 L3: 18 MB I+D on chip per chip

 Other: None

Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2933)

Storage: 1 x 800 GB SAS SSD, RAID 0

Other: None

Software

OS: Red Hat Enterprise Linux 8.3 (Ootpa)
Kernel 4.18.0-240.el8.x86_64

Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux

Parallel: Yes

Firmware: HPE BIOS Version I44 v1.54 11/03/2021 released Nov-2021

File System: xfs

System State: Run level 3 (multi-user)

Base Pointers: 64-bit

Peak Pointers: 64-bit

Other: jemalloc memory allocator V5.0.1

Power Management: BIOS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base						Peak					
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	24	243	7.32	245	7.24	**243**	**7.29**	24	210	8.43	211	8.41	**211**	**8.42**
602.gcc_s	24	**377**	**10.6**	377	10.6	377	10.5	24	366	10.9	364	10.9	**364**	**10.9**
605.mcf_s	24	238	19.8	**238**	**19.8**	239	19.7	24	238	19.8	**238**	**19.8**	239	19.7
620.omnetpp_s	24	190	8.59	**189**	**8.64**	188	8.67	24	190	8.59	**189**	**8.64**	188	8.67
623.xalancbmk_s	24	103	13.7	**104**	**13.6**	104	13.6	24	103	13.7	**104**	**13.6**	104	13.6
625.x264_s	24	104	17.0	**104**	**16.9**	104	16.9	24	**100**	**17.6**	99.9	17.7	100	17.6
631.deepsjeng_s	24	236	6.07	237	6.06	**236**	**6.06**	24	236	6.07	237	6.06	**236**	**6.06**
641.leela_s	24	342	4.99	342	4.99	**342**	**4.99**	24	342	4.99	342	4.99	**342**	**4.99**
648.exchange2_s	24	148	19.9	**148**	**19.9**	147	19.9	24	148	19.9	**148**	**19.9**	147	19.9
657.xz_s	24	**291**	**21.2**	289	21.4	291	21.2	24	**291**	**21.2**	289	21.4	291	21.2
SPECspeed®2017_int_base =		**11.5**										
SPECspeed®2017_int_peak =								**11.7**				

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>        /proc/sys/vm/drop_caches
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"
```

General Notes

```
 Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
 memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
```

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Tested by:	HPE	**Software Availability:**	Dec-2020

General Notes (Continued)

sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Submitted_by: "Bucek, James" <james.bucek@hpe.com>
Submitted: Wed Jan 12 10:02:51 EST 2022
Submission: cpu2017-20220103-30708.sub

Platform Notes

```
BIOS Configuration:
 Workload Profile set to General Peak Frequency Compute
 Intel Hyper-Threading set to Disabled
 Thermal Configuration set to Maximum Cooling
 Memory Patrol Scrubbing set to Disabled
 Advanced Memory Protection set to Advanced ECC
 Last Level Cache (LLC) Prefetch set to Enabled
 Last Level Cache (LLC) Dead Line Allocation set to Disabled
 Enhanced Processor Performance set to Enabled
 Workload Profile set to Custom
     Energy/Performance Bias set to Balanced Power
     DCU Stream Prefetcher set to Disabled
     Adjacent Sector Prefetch set to Disabled
     Minimum Processor Idle Power Package C-State set to No Package State
     Numa Group Size Optimization set to Flat

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on localhost.localdomain Fri Dec 10 21:08:50 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
     https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
       2  "physical id"s (chips)
       24 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 12
       siblings  : 12
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11

 From lscpu from util-linux 2.32.1:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
```

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Tested by:	HPE	**Software Availability:**	Dec-2020

Platform Notes (Continued)

```
         Byte Order:          Little Endian
         CPU(s):              24
         On-line CPU(s) list: 0-23
         Thread(s) per core:  1
         Core(s) per socket:  12
         Socket(s):           2
         NUMA node(s):        2
         Vendor ID:           GenuineIntel
         CPU family:          6
         Model:               106
         Model name:          Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
         Stepping:            6
         CPU MHz:             2618.177
         BogoMIPS:            6000.00
         Virtualization:      VT-x
         L1d cache:           48K
         L1i cache:           32K
         L2 cache:            1280K
         L3 cache:            18432K
         NUMA node0 CPU(s):   0-11
         NUMA node1 CPU(s):   12-23
         Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
     pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
     lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
     aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
     xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
     avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
     mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
     fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq
     rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw
     avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
     cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts avx512vbmi umip pku
     ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme
     avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

  /proc/cpuinfo cache data
     cache size : 18432 KB

  From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
     available: 2 nodes (0-1)
     node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
     node 0 size: 1013880 MB
     node 0 free: 1030894 MB
     node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
     node 1 size: 1013039 MB
     node 1 free: 1031659 MB
```

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CPU2017 License: 3		**Test Date:**	Dec-2021
Test Sponsor:	HPE	**Hardware Availability:**	Nov-2021
Tested by:	HPE	**Software Availability:**	Dec-2020

Platform Notes (Continued)

```
   node distances:
   node   0   1
     0:  10  20
     1:  20  10

 From /proc/meminfo
    MemTotal:       2113497044 kB
    HugePages_Total:        0
    Hugepagesize:       2048 kB

 /sbin/tuned-adm active
     Current active profile: throughput-performance

 From /etc/*release* /etc/*version*
    os-release:
       NAME="Red Hat Enterprise Linux"
       VERSION="8.3 (Ootpa)"
       ID="rhel"
       ID_LIKE="fedora"
       VERSION_ID="8.3"
       PLATFORM_ID="platform:el8"
       PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
       ANSI_COLOR="0;31"
    redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
    system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
    system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga

 uname -a:
    Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
    x86_64 x86_64 x86_64 GNU/Linux

 Kernel self-reported vulnerability status:

 CVE-2018-12207 (iTLB Multihit):                   Not affected
 CVE-2018-3620 (L1 Terminal Fault):                Not affected
 Microarchitectural Data Sampling:                 Not affected
 CVE-2017-5754 (Meltdown):                         Not affected
 CVE-2018-3639 (Speculative Store Bypass):         Mitigation: Speculative Store
                                                   Bypass disabled via prctl and
                                                   seccomp
 CVE-2017-5753 (Spectre variant 1):                Mitigation: usercopy/swapgs
                                                   barriers and __user pointer
                                                   sanitization
 CVE-2017-5715 (Spectre variant 2):                Mitigation: Enhanced IBRS, IBPB:
                                                   conditional, RSB filling
 CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
 CVE-2019-11135 (TSX Asynchronous Abort):          Not affected
```

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Platform Notes (Continued)

```
  run-level 3 Dec 10 21:07

  SPEC is set to: /home/cpu2017
     Filesystem              Type   Size  Used Avail Use% Mounted on
     /dev/mapper/rhel-home xfs    670G  110G  561G  17% /home

  From /sys/devices/virtual/dmi/id
     Vendor:          HPE
     Product:         Synergy 480 Gen10 Plus
     Product Family: Synergy
     Serial:          CN70330Q5F


  Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
  interpret this section. The 'dmidecode' program reads system data which is "intended to
  allow hardware to be accurately determined", but the intent may not be met, as there are
  frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
      32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200, configured at 2933

  BIOS:
     BIOS Vendor:         HPE
     BIOS Version:        I44
     BIOS Date:           11/03/2021
     BIOS Revision:       1.54
     Firmware Revision: 2.40

  (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C        | 600.perlbench_s(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
         | 625.x264_s(base, peak) 657.xz_s(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

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Compiler Version Notes (Continued)

```
--------------------------------------------------------------------------------

================================================================================
C        | 600.perlbench_s(peak)
--------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------

================================================================================
C        | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
         | 625.x264_s(base, peak) 657.xz_s(base, peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

================================================================================
C++      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
         | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

================================================================================
Fortran | 648.exchange2_s(base, peak)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

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Base Portability Flags

600.perlbench_s: `-DSPEC_LP64 -DSPEC_LINUX_X64`
602.gcc_s: `-DSPEC_LP64`
605.mcf_s: `-DSPEC_LP64`
620.omnetpp_s: `-DSPEC_LP64`
623.xalancbmk_s: `-DSPEC_LP64 -DSPEC_LINUX`
625.x264_s: `-DSPEC_LP64`
631.deepsjeng_s: `-DSPEC_LP64`
641.leela_s: `-DSPEC_LP64`
648.exchange2_s: `-DSPEC_LP64`
657.xz_s: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
```
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

C++ benchmarks:
```
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc
```

Fortran benchmarks:
```
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
```

Peak Compiler Invocation

C benchmarks (except as noted below):
`icx`

 600.perlbench_s: `icc`

C++ benchmarks:
`icpx`

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Peak Compiler Invocation (Continued)

Fortran benchmarks:
`ifort`

Peak Portability Flags

`Same as Base Portability Flags`

Peak Optimization Flags

C benchmarks:

600.perlbench_s: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2)
`-xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=4 -fno-strict-overflow`
`-mbranches-within-32B-boundaries`
`-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

602.gcc_s: `-m64 -std=c11 -Wl,-z,muldefs` -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) `-xCORE-AVX512 -flto`
-Ofast(pass 1) `-O3 -ffast-math -qopt-mem-layout-trans=4`
`-mbranches-within-32B-boundaries`
`-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

605.mcf_s: basepeak = yes

625.x264_s: `-DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs`
`-xCORE-AVX512 -flto -O3 -ffast-math`
`-qopt-mem-layout-trans=4 -fno-alias`
`-mbranches-within-32B-boundaries`
`-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

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Peak Optimization Flags (Continued)

641.leela_s: `basepeak = yes`

Fortran benchmarks:

648.exchange2_s: `basepeak = yes`

The flags files that were used to format this result can be browsed at
`http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html`
`http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.html`

You can also download the XML flags sources by saving the following links:
`http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml`
`http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.xml`

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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