



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECrate®2017_int_base = 145

SPECrate®2017_int_peak = 150

CPU2017 License: 9019

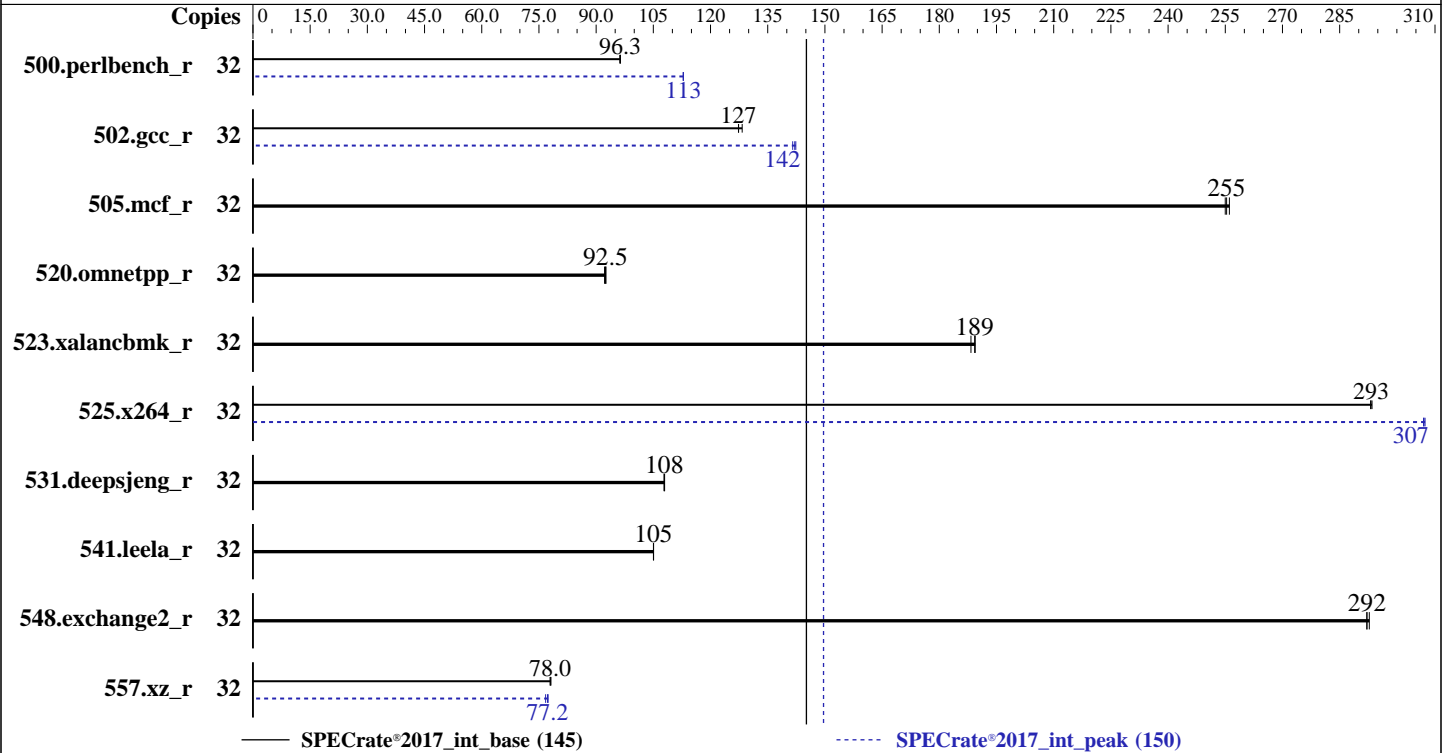
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2021

Hardware Availability: Jun-2021

Software Availability: Dec-2020



Hardware

CPU Name: Intel Xeon Gold 6334
 Max MHz: 3700
 Nominal: 3600
 Enabled: 16 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 1.25 MB I+D on chip per core
 L3: 18 MB I+D on chip per chip
 Other: None
 Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R)
 Storage: 1 x 240 GB SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
 Parallel: No
 Firmware: Version 4.2.1d released Jul-2021
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	32	529	96.4	530	96.2	<u>529</u>	<u>96.3</u>	32	451	113	<u>451</u>	<u>113</u>	451	113
502.gcc_r	32	356	127	353	128	<u>356</u>	<u>127</u>	32	<u>319</u>	<u>142</u>	320	142	318	142
505.mcf_r	32	203	255	202	256	<u>203</u>	<u>255</u>	32	203	255	202	256	<u>203</u>	<u>255</u>
520.omnetpp_r	32	<u>454</u>	<u>92.5</u>	455	92.2	453	92.6	32	<u>454</u>	<u>92.5</u>	455	92.2	453	92.6
523.xalancbmk_r	32	178	189	<u>179</u>	<u>189</u>	179	188	32	178	189	<u>179</u>	<u>189</u>	179	188
525.x264_r	32	191	293	<u>191</u>	<u>293</u>	191	293	32	183	307	182	307	<u>182</u>	<u>307</u>
531.deepsjeng_r	32	340	108	340	108	<u>340</u>	<u>108</u>	32	340	108	340	108	<u>340</u>	<u>108</u>
541.leela_r	32	504	105	505	105	<u>505</u>	<u>105</u>	32	504	105	505	105	<u>505</u>	<u>105</u>
548.exchange2_r	32	287	292	286	293	<u>287</u>	<u>292</u>	32	287	292	286	293	<u>287</u>	<u>292</u>
557.xz_r	32	442	78.2	443	78.0	<u>443</u>	<u>78.0</u>	32	450	76.7	446	77.4	<u>447</u>	<u>77.2</u>

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)



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General Notes (Continued)

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Adjacent Cache Line Prefetcher set to Disabled

DCU Streamer Prefetch set to Disabled

UPI Link Enablement set to 1

UPI Power Management set to Enabled

Sub NUMA Clustering set to Enabled

LLC Dead Line set to Disabled

Memory Refresh Rate set to 1x Refresh

ADDDC Sparing set to Disabled

Patrol Scrub set to Disabled

Energy Efficient Turbo set to Enabled

Processor C6 Report set to Enabled

Processor C1E set to Enabled

```
Sysinfo program /home/cpu2017/bin/sysinfo
```

```
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
```

```
running on localhost Mon Aug 23 02:30:29 2021
```

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
```

```
model name : Intel(R) Xeon(R) Gold 6334 CPU @ 3.60GHz
```

```
2 "physical id"s (chips)
```

```
32 "processors"
```

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 8
```

```
siblings : 16
```

```
physical 0: cores 0 1 2 3 4 5 6 7
```

```
physical 1: cores 0 1 2 3 4 5 6 7
```

(Continued on next page)



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Platform Notes (Continued)

```

From lscpu from util-linux 2.33.1:
Architecture:          x86_64
CPU op-mode(s):       32-bit, 64-bit
Byte Order:           Little Endian
Address sizes:        46 bits physical, 57 bits virtual
CPU(s):               32
On-line CPU(s) list:  0-31
Thread(s) per core:   2
Core(s) per socket:   8
Socket(s):            2
NUMA node(s):        4
Vendor ID:            GenuineIntel
CPU family:           6
Model:                106
Model name:           Intel(R) Xeon(R) Gold 6334 CPU @ 3.60GHz
Stepping:             6
CPU MHz:              800.296
CPU max MHz:          3700.0000
CPU min MHz:          800.0000
BogoMIPS:             7200.00
Virtualization:      VT-x
L1d cache:           48K
L1i cache:           32K
L2 cache:            1280K
L3 cache:            18432K
NUMA node0 CPU(s):   0-3,16-19
NUMA node1 CPU(s):   4-7,20-23
NUMA node2 CPU(s):   8-11,24-27
NUMA node3 CPU(s):   12-15,28-31
Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

/proc/cpuinfo cache data
cache size : 18432 KB

```

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Platform Notes (Continued)

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 16 17 18 19
node 0 size: 257638 MB
node 0 free: 257362 MB
node 1 cpus: 4 5 6 7 20 21 22 23
node 1 size: 258045 MB
node 1 free: 257659 MB
node 2 cpus: 8 9 10 11 24 25 26 27
node 2 size: 258045 MB
node 2 free: 257646 MB
node 3 cpus: 12 13 14 15 28 29 30 31
node 3 size: 258009 MB
node 3 free: 257784 MB
node distances:
node  0  1  2  3
  0:  10  11  20  20
  1:  11  10  20  20
  2:  20  20  10  11
  3:  20  20  11  10
```

From /proc/meminfo

```
MemTotal:      1056501436 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*

```
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"
```

uname -a:

```
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multihit):	Not affected
CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):	Not affected
CVE-2019-11135 (TSX Asynchronous Abort):	Not affected

run-level 3 Aug 23 02:26

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda2	btrfs	222G	31G	190G	14%	/home

```
From /sys/devices/virtual/dmi/id
Vendor:          Cisco Systems Inc
Product:         UCSC-C220-M6S
Serial:          WZP24430ADF
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

```
BIOS:
  BIOS Vendor:      Cisco Systems, Inc.
  BIOS Version:     C220M6.4.2.1d.0.0730210924
  BIOS Date:        07/30/2021
  BIOS Revision:    5.22
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C      | 500.perlbench_r(peak) 557.xz_r(peak)
=====
```

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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C | 500.perlbench_r(peak) 557.xz_r(peak)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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=====
C | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
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=====
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base)

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Compiler Version Notes (Continued)

=====
C | 500.perlbench_r(peak) 557.xz_r(peak)

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=====
C | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
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=====
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++ | 520.omnetpp_r(base, peak) 523.xalanbmk_r(base, peak)
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Base Compiler Invocation

C benchmarks:
icx

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Base Compiler Invocation (Continued)

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
```

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Base Optimization Flags (Continued)

Fortran benchmarks (continued):

-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):

icx

500.perlbench_r: icc

557.xz_r: icc

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

502.gcc_r: -D_FILE_OFFSET_BITS=64

505.mcf_r: -DSPEC_LP64

520.omnetpp_r: -DSPEC_LP64

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX

525.x264_r: -DSPEC_LP64

531.deepsjeng_r: -DSPEC_LP64

541.leela_r: -DSPEC_LP64

548.exchange2_r: -DSPEC_LP64

557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)

-xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4 -fno-strict-overflow

-mbranches-within-32B-boundaries

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin

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Peak Optimization Flags (Continued)

500.perlbench_r (continued):

-lqkmalloc

502.gcc_r: -m32

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin

-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)

-fprofile-use=default.profddata(pass 2) -xCORE-AVX512 -flto

-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4

-mbranches-within-32B-boundaries

-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto

-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias

-mbranches-within-32B-boundaries

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin

-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin

-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revG.html>

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revG.xml>



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Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECrate®2017_int_base = 145

SPECrate®2017_int_peak = 150

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2021

Hardware Availability: Jun-2021

Software Availability: Dec-2020

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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