



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

PowerEdge MX740 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECrate®2017_int_base = 119

SPECrate®2017_int_peak = 122

CPU2017 License: 55

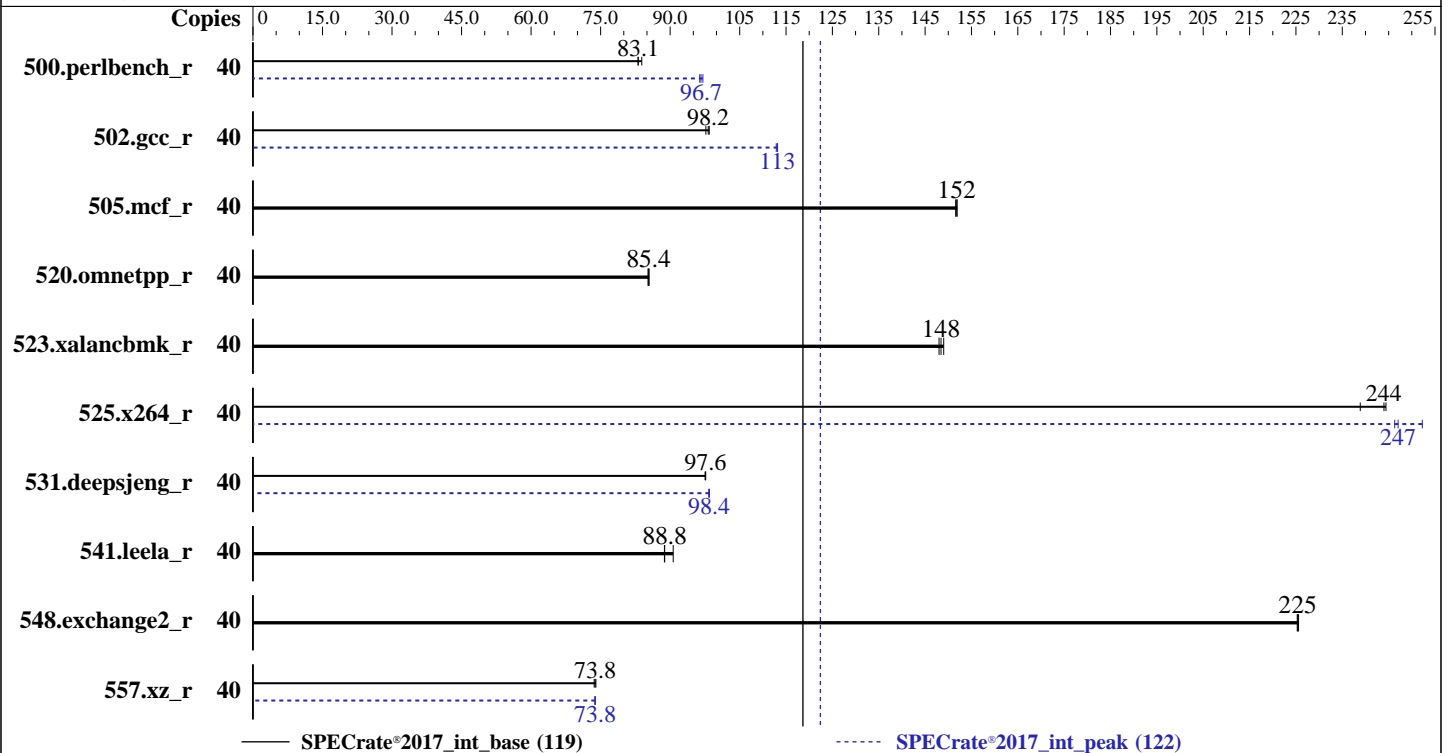
Test Sponsor: Dell Inc.

Tested by: Dell Inc.

Test Date: Apr-2020

Hardware Availability: Feb-2020

Software Availability: Nov-2019



Hardware

CPU Name: Intel Xeon Silver 4210R
 Max MHz: 3200
 Nominal: 2400
 Enabled: 20 cores, 2 chips, 2 threads/core
 Orderable: 1,2 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 13.75 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx8 PC4-2933V-R, running at 2400)
 Storage: 1 x 480 GB SATA SSD
 Other: None

Software

OS: Red Hat Enterprise Linux 8.1
 kernel 4.18.0-147.el8.x86_64
 Compiler: C/C++: Version 19.0.5.281 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.5.281 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 2.7.1 released Feb-2020
 File System: tmpfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	40	759	83.9	766	83.1	766	83.1	40	656	97.1	661	96.4	659	96.7
502.gcc_r	40	575	98.4	577	98.2	580	97.7	40	501	113	502	113	500	113
505.mcf_r	40	426	152	426	152	426	152	40	426	152	426	152	426	152
520.omnetpp_r	40	615	85.4	616	85.2	614	85.4	40	615	85.4	616	85.2	614	85.4
523.xalancbmk_r	40	285	148	283	149	285	148	40	285	148	283	149	285	148
525.x264_r	40	293	239	287	244	287	244	40	284	247	284	246	278	252
531.deepsjeng_r	40	470	97.6	469	97.7	470	97.5	40	466	98.4	465	98.5	466	98.4
541.leela_r	40	746	88.8	746	88.8	731	90.7	40	746	88.8	746	88.8	731	90.7
548.exchange2_r	40	465	225	465	225	465	226	40	465	225	465	225	465	226
557.xz_r	40	584	74.0	587	73.6	585	73.8	40	586	73.8	585	73.8	585	73.8

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/dev/shm/cpu2017/lib/intel64:/dev/shm/cpu2017/lib/ia32:/dev/shm/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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General Notes (Continued)

is mitigated in the system as tested and documented.
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
`sync; echo 3> /proc/sys/vm/drop_caches`
 runcpu command invoked through numactl i.e.:
`numactl --interleave=all runcpu <etc>`
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS settings:
 Virtualization Technology disabled
 DCU Streamer Prefetcher disabled
 System Profile set to Custom
 CPU Performance set to Maximum Performance
 C States set to Autonomous
 C1E disabled
 Uncore Frequency set to Dynamic
 Energy Efficiency Policy set to Performance
 Memory Patrol Scrub disabled
 Logical Processor enabled
 CPU Interconnect Bus Link Power Management enabled
 PCI ASPM L1 Link Power Management enabled

Sysinfo program /dev/shm/cpu2017/bin/sysinfo
 Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
 running on localhost.localdomain Fri May 1 12:41:48 2020

SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```

model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
 2 "physical id"s (chips)
 40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

```

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Platform Notes (Continued)

From lscpu:

```

Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 40
On-line CPU(s) list:   0-39
Thread(s) per core:    2
Core(s) per socket:    10
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping:               7
CPU MHz:                1070.960
CPU max MHz:           3200.0000
CPU min MHz:           1000.0000
BogoMIPS:               4800.00
Virtualization:        VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               14080K
NUMA node0 CPU(s):     0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38
NUMA node1 CPU(s):     1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx fl6c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
arch_capabilities

```

/proc/cpuinfo cache data
cache size : 14080 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
node 0 size: 385583 MB

```

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Platform Notes (Continued)

```

node 0 free: 367501 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
node 1 size: 387067 MB
node 1 free: 360293 MB
node distances:
node    0    1
  0:   10   21
  1:   21   10

```

```

From /proc/meminfo
MemTotal:          791194144 kB
HugePages_Total:      0
Hugepagesize:       2048 kB

```

```

From /etc/*release* /etc/*version*
os-release:
NAME="Red Hat Enterprise Linux"
VERSION="8.1 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.1"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

```

```

uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

```

CVE-2018-3620 (L1 Terminal Fault):          Not affected
Microarchitectural Data Sampling:          Not affected
CVE-2017-5754 (Meltdown):                  Not affected
CVE-2018-3639 (Speculative Store Bypass):  Mitigation: Speculative Store Bypass disabled
                                              via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):         Mitigation: usercopy/swapgs barriers and __user
                                              pointer sanitization
CVE-2017-5715 (Spectre variant 2):         Mitigation: Enhanced IBRS, IBPB: conditional,
                                              RSB filling

```

run-level 3 Apr 28 15:03

SPEC is set to: /dev/shm/cpu2017

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Platform Notes (Continued)

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
tmpfs	tmpfs	378G	33G	345G	9%	/dev/shm

```

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.1 02/14/2020
Vendor: Dell Inc.
Product: PowerEdge MX740c
Product Family: PowerEdge
Serial: 1234567

```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```

Memory:
 21x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
 1x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
 2x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933

```

(End of data from sysinfo program)

Compiler Version Notes

```

=====
C      | 502.gcc_r(peak)
-----
Intel(R) C Compiler for applications running on IA-32, Version 19.0.5 NextGen
  Technology Build 20190729
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----

```

```

=====
C      | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
      | 525.x264_r(base, peak) 557.xz_r(base)
-----
Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.0.5
  NextGen Technology Build 20190729
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----

```

```

=====
C      | 500.perlbench_r(peak) 557.xz_r(peak)
-----
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```

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Compiler Version Notes (Continued)

=====
C | 502.gcc_r(peak)
=====

Intel(R) C Compiler for applications running on IA-32, Version 19.0.5 NextGen
Technology Build 20190729
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
=====

Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.0.5
NextGen Technology Build 20190729
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
C | 500.perlbench_r(peak) 557.xz_r(peak)
=====

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
C | 502.gcc_r(peak)
=====

Intel(R) C Compiler for applications running on IA-32, Version 19.0.5 NextGen
Technology Build 20190729
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
=====

Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.0.5
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=====
C | 500.perlbench_r(peak) 557.xz_r(peak)
=====

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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```
=====  
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)  
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)  
=====
```

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 19.0.5 NextGen Technology Build 20190729
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```
=====  
Fortran  | 548.exchange2_r(base, peak)  
=====
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64

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Base Portability Flags (Continued)

548.exchange2_r: -DSPEC_LP64

557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -flto -mfpmath=sse  
-funroll-loops -qnextgen -fuse-ld=gold -qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin  
-lqkmallo
```

C++ benchmarks:

```
-m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -flto -mfpmath=sse  
-funroll-loops -qnextgen -fuse-ld=gold -qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin  
-lqkmallo
```

Fortran benchmarks:

```
-m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ipo -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin  
-lqkmallo
```

Peak Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

502.gcc_r: -D_FILE_OFFSET_BITS=64

505.mcf_r: -DSPEC_LP64

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Peak Portability Flags (Continued)

```

520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

```

Peak Optimization Flags

C benchmarks:

```

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin
-lqkmalloc

```

```

502.gcc_r: -m32
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profddata(pass 2) -xCORE-AVX2 -flto
-Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib
-ljemalloc

```

505.mcf_r: basepeak = yes

```

525.x264_r: -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -flto -O3
-ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin
-lqkmalloc

```

```

557.xz_r: -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin
-lqkmalloc

```

C++ benchmarks:

520.omnetpp_r: basepeak = yes

(Continued on next page)



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Peak Optimization Flags (Continued)

523.xalancbmk_r: basepeak = yes

```
531.deepsjeng_r: -m64 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -flto
-Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.5.281/linux/compiler/lib/intel64_lin
-lqkmalloc
```

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic19.0u5-official-linux64_revD.html

<http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE9.html>

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.0u5-official-linux64_revD.xml

<http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE9.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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