



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPECrate®2017\_fp\_base = 414

SPECrate®2017\_fp\_peak = Not Run

CPU2017 License: 9019

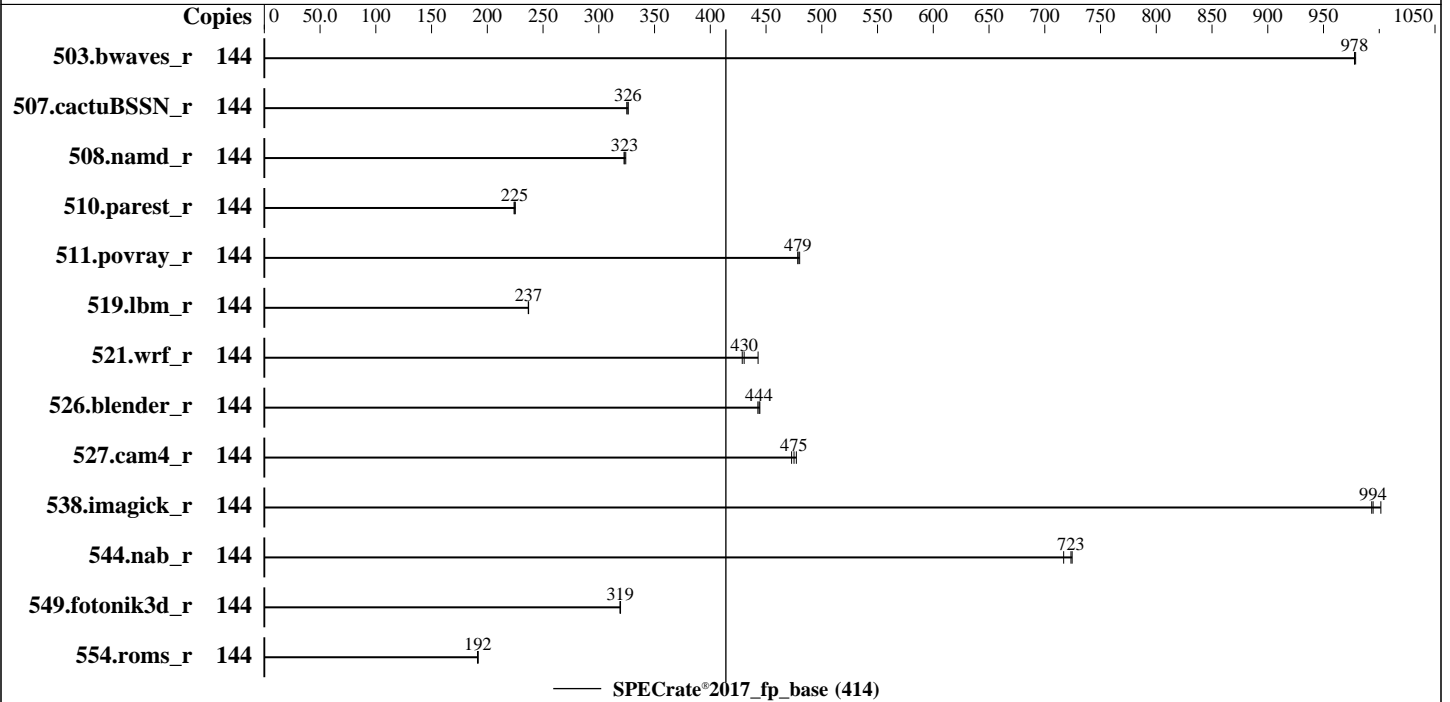
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 6240L  
 Max MHz: 3900  
 Nominal: 2600  
 Enabled: 72 cores, 4 chips, 2 threads/core  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 300 GB 15K RPM SAS HDD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-25.28-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4g released Jul-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: None  
 Power Management: default



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	144	1475	979	1477	978	<b>1477</b>	<b>978</b>							
507.cactuBSSN_r	144	559	326	561	325	<b>559</b>	<b>326</b>							
508.namd_r	144	<b>423</b>	<b>323</b>	424	323	422	324							
510.parest_r	144	<b>1677</b>	<b>225</b>	1682	224	1674	225							
511.povray_r	144	<b>702</b>	<b>479</b>	703	479	700	480							
519.lbm_r	144	<b>641</b>	<b>237</b>	641	237	640	237							
521.wrf_r	144	753	429	728	443	<b>750</b>	<b>430</b>							
526.blender_r	144	495	443	493	444	<b>494</b>	<b>444</b>							
527.cam4_r	144	533	473	<b>530</b>	<b>475</b>	528	477							
538.imagick_r	144	<b>360</b>	<b>994</b>	358	1000	361	993							
544.nab_r	144	<b>335</b>	<b>723</b>	338	717	334	725							
549.fotonik3d_r	144	<b>1758</b>	<b>319</b>	1756	319	1758	319							
554.roms_r	144	1194	192	<b>1194</b>	<b>192</b>	1197	191							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches

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### General Notes (Continued)

runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
running on linux-75co Sun Oct 27 04:15:00 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Gold 6240L CPU @ 2.60GHz  
4 "physical id"s (chips)  
144 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 18  
siblings : 36  
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27  
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27  
physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27  
physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:  
Architecture: x86\_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 144  
On-line CPU(s) list: 0-143  
Thread(s) per core: 2  
Core(s) per socket: 18

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### Platform Notes (Continued)

```

Socket(s): 4
NUMA node(s): 8
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240L CPU @ 2.60GHz
Stepping: 7
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,72-74,77,78,81,82,86,87
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,75,76,79,80,83-85,88,89
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,90-92,95,96,99,100,104,105
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,93,94,97,98,101-103,106,107
NUMA node4 CPU(s): 36-38,41,42,45,46,50,51,108-110,113,114,117,118,122,123
NUMA node5 CPU(s): 39,40,43,44,47-49,52,53,111,112,115,116,119-121,124,125
NUMA node6 CPU(s): 54-56,59,60,63,64,68,69,126-128,131,132,135,136,140,141
NUMA node7 CPU(s): 57,58,61,62,65-67,70,71,129,130,133,134,137-139,142,143
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni flush_l1d arch_capabilities

```

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 2 5 6 9 10 14 15 72 73 74 77 78 81 82 86 87
node 0 size: 192100 MB
node 0 free: 191799 MB
node 1 cpus: 3 4 7 8 11 12 13 16 17 75 76 79 80 83 84 85 88 89

```

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### Platform Notes (Continued)

```

node 1 size: 193532 MB
node 1 free: 193282 MB
node 2 cpus: 18 19 20 23 24 27 28 32 33 90 91 92 95 96 99 100 104 105
node 2 size: 193532 MB
node 2 free: 193160 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 93 94 97 98 101 102 103 106 107
node 3 size: 193532 MB
node 3 free: 193295 MB
node 4 cpus: 36 37 38 41 42 45 46 50 51 108 109 110 113 114 117 118 122 123
node 4 size: 193532 MB
node 4 free: 193334 MB
node 5 cpus: 39 40 43 44 47 48 49 52 53 111 112 115 116 119 120 121 124 125
node 5 size: 193532 MB
node 5 free: 193343 MB
node 6 cpus: 54 55 56 59 60 63 64 68 69 126 127 128 131 132 135 136 140 141
node 6 size: 193503 MB
node 6 free: 193238 MB
node 7 cpus: 57 58 61 62 65 66 67 70 71 129 130 133 134 137 138 139 142 143
node 7 size: 193530 MB
node 7 free: 193333 MB
node distances:
node  0  1  2  3  4  5  6  7
  0:  10 11 21 21 21 21 21 21
  1:  11 10 21 21 21 21 21 21
  2:  21 21 10 11 21 21 21 21
  3:  21 21 11 10 21 21 21 21
  4:  21 21 21 21 10 11 21 21
  5:  21 21 21 21 11 10 21 21
  6:  21 21 21 21 21 21 10 11
  7:  21 21 21 21 21 21 11 10

```

From /proc/meminfo

MemTotal: 1583920180 kB

HugePages\_Total: 0

Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*

os-release:

NAME="SLES"

VERSION="15"

VERSION\_ID="15"

PRETTY\_NAME="SUSE Linux Enterprise Server 15"

ID="sles"

ID\_LIKE="suse"

ANSI\_COLOR="0;32"

CPE\_NAME="cpe:/o:suse:sles:15"

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### Platform Notes (Continued)

```
uname -a:
Linux linux-75co 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault):          Not affected
Microarchitectural Data Sampling:         No status reported
CVE-2017-5754 (Meltdown):                  Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                              via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):         Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):         Mitigation: Enhanced IBRS, IBPB: conditional,
                                              RSB filling
```

```
run-level 3 Oct 27 04:14
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda3       xfs   177G   69G  109G   39% /home
```

```
From /sys/devices/virtual/dmi/id
BIOS:      Cisco Systems, Inc. C480M5.4.0.4g.0.0712190013 07/12/2019
Vendor:    Cisco Systems Inc
Product:   UCSC-C480-M5
Serial:    FCH2223W00A
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(End of data from sysinfo program)

### Compiler Version Notes

```
=====
C          | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-----
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

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### Compiler Version Notes (Continued)

=====  
C++ | 508.namd\_r(base) 510.parest\_r(base)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++, C, Fortran | 507.cactuBSSN\_r(base)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 503.bwaves\_r(base) 549.fotonik3d\_r(base) 554.roms\_r(base)  
-----

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base)  
-----

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
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## Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```





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## Base Optimization Flags

### C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

### C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

### Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

### Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

### Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

### Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>

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