



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

CPU2017 License: 9019

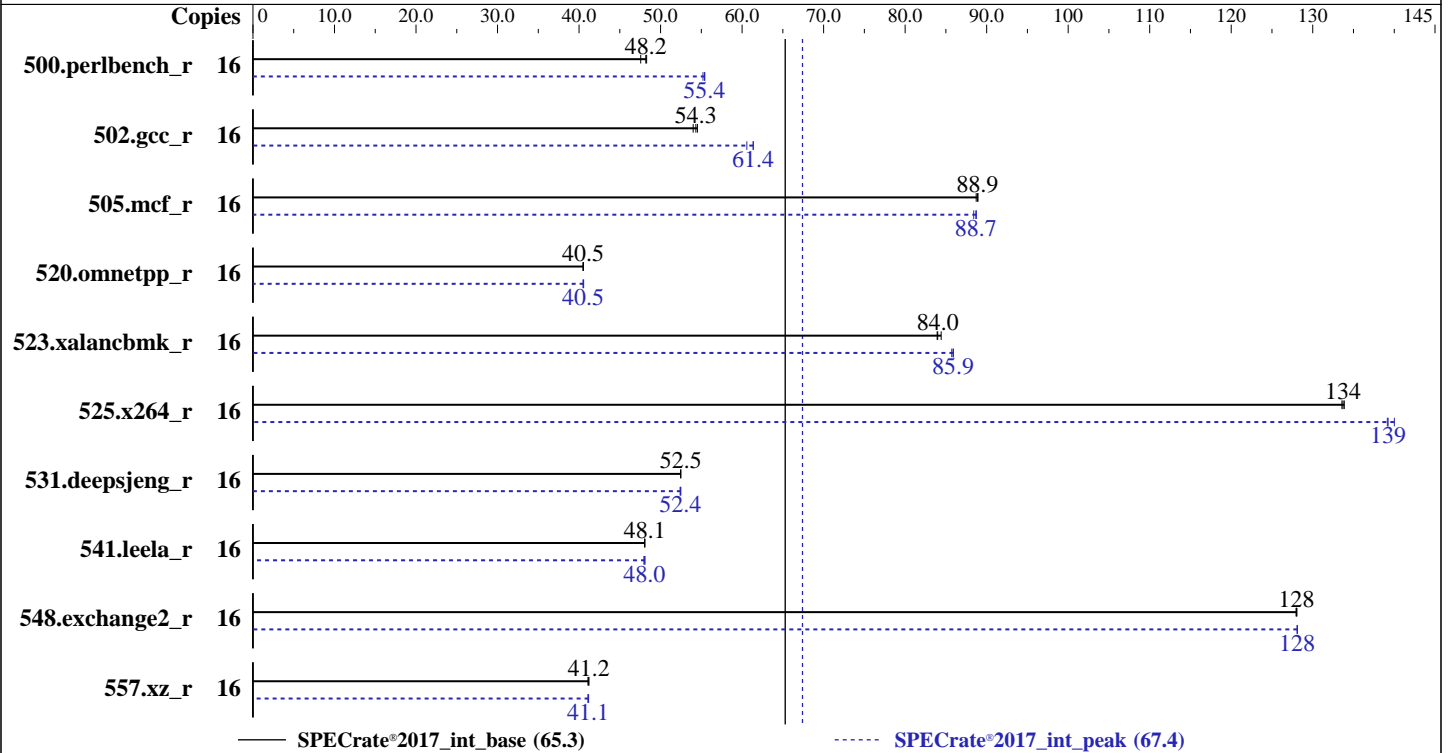
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Sep-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 5222  
 Max MHz: 3900  
 Nominal: 3800  
 Enabled: 8 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 16.5 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 1.9 TB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4g released Jul-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: --



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	16	<u>529</u>	<u>48.2</u>	536	47.6	527	48.3	16	460	55.4	461	55.2	<u>460</u>	<u>55.4</u>
502.gcc_r	16	420	54.0	416	54.5	<u>417</u>	<u>54.3</u>	16	<u>369</u>	<u>61.4</u>	369	61.4	374	60.6
505.mcf_r	16	<u>291</u>	<u>88.9</u>	291	88.7	291	88.9	16	<u>292</u>	<u>88.7</u>	292	88.4	291	88.7
520.omnetpp_r	16	<u>518</u>	<u>40.5</u>	518	40.5	519	40.5	16	518	40.5	517	40.6	<u>518</u>	<u>40.5</u>
523.xalancbmk_r	16	<u>201</u>	<u>84.0</u>	200	84.4	201	83.9	16	197	85.9	197	85.7	<u>197</u>	<u>85.9</u>
525.x264_r	16	209	134	<u>210</u>	<u>134</u>	210	134	16	200	140	<u>201</u>	<u>139</u>	201	139
531.deepsjeng_r	16	349	52.5	<u>349</u>	<u>52.5</u>	349	52.5	16	350	52.4	<u>350</u>	<u>52.4</u>	349	52.5
541.leela_r	16	<u>551</u>	<u>48.1</u>	551	48.0	551	48.1	16	551	48.1	<u>552</u>	<u>48.0</u>	553	48.0
548.exchange2_r	16	<u>328</u>	<u>128</u>	328	128	327	128	16	<u>327</u>	<u>128</u>	327	128	327	128
557.xz_r	16	419	41.2	421	41.1	<u>420</u>	<u>41.2</u>	16	<u>420</u>	<u>41.1</u>	420	41.2	420	41.1

SPECrate®2017\_int\_base = **65.3**

SPECrate®2017\_int\_peak = **67.4**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

### General Notes (Continued)

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

### Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9

running on linux-jm4k Fri Sep 20 08:30:19 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz

2 "physical id"s (chips)

16 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 4

siblings : 8

physical 0: cores 2 4 5 9

physical 1: cores 5 8 9 13

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 16

On-line CPU(s) list: 0-15

Thread(s) per core: 2

Core(s) per socket: 4

Socket(s): 2

NUMA node(s): 4

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

Model name: Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz

Stepping: 6

CPU MHz: 3800.000

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```

CPU max MHz:          3900.0000
CPU min MHz:          1200.0000
BogoMIPS:             7600.00
Virtualization:       VT-x
L1d cache:            32K
L1i cache:            32K
L2 cache:             1024K
L3 cache:             16896K
NUMA node0 CPU(s):   0,3,8,11
NUMA node1 CPU(s):   1,2,9,10
NUMA node2 CPU(s):   4,7,12,15
NUMA node3 CPU(s):   5,6,13,14
Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 16896 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 3 8 11
node 0 size: 192106 MB
node 0 free: 191756 MB
node 1 cpus: 1 2 9 10
node 1 size: 193530 MB
node 1 free: 193322 MB
node 2 cpus: 4 7 12 15
node 2 size: 193500 MB
node 2 free: 193310 MB
node 3 cpus: 5 6 13 14
node 3 size: 193530 MB
node 3 free: 193296 MB
node distances:
node  0  1  2  3
0:   10  11  21  21
1:   11  10  21  21

```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```
2: 21 21 10 11
3: 21 21 11 10
```

```
From /proc/meminfo
MemTotal:      791212300 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-jm4k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation,
IBPB, IBRS_FW
```

```
run-level 3 Sep 20 08:29
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdb1       xfs   224G   20G  204G   9% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(End of data from sysinfo program)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Sep-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Compiler Version Notes

=====  
C | 502.gcc\_r(peak)  
-----

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base, peak) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 502.gcc\_r(peak)  
-----

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base, peak) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 523.xalanbmk\_r(peak)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalanbmk\_r(base)  
531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
C++ | 523.xalancbmk\_r(peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base)  
| 531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
Fortran | 548.exchange2\_r(base, peak)

-----  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

C++ benchmarks:  
icpc -m64

Fortran benchmarks:  
ifort -m64

## Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Base Portability Flags (Continued)

```
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

(Continued on next page)





# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 5222,  
3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Peak Compiler Invocation (Continued)

Fortran benchmarks:

ifort -m64

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECrate®2017\_int\_base = 65.3

SPECrate®2017\_int\_peak = 67.4

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc

523.xalancbmk\_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo

-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4

-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng\_r: Same as 520.omnetpp\_r

541.leela\_r: Same as 520.omnetpp\_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-19 23:00:18-0400.

Report generated on 2020-07-13 18:39:38 by CPU2017 PDF formatter v6255.

Originally published on 2019-11-04.