



SPEC® CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6144 3.50 GHz)

SPECrate2017_fp_base = 276

SPECrate2017_fp_peak = 282

CPU2017 License: 9019

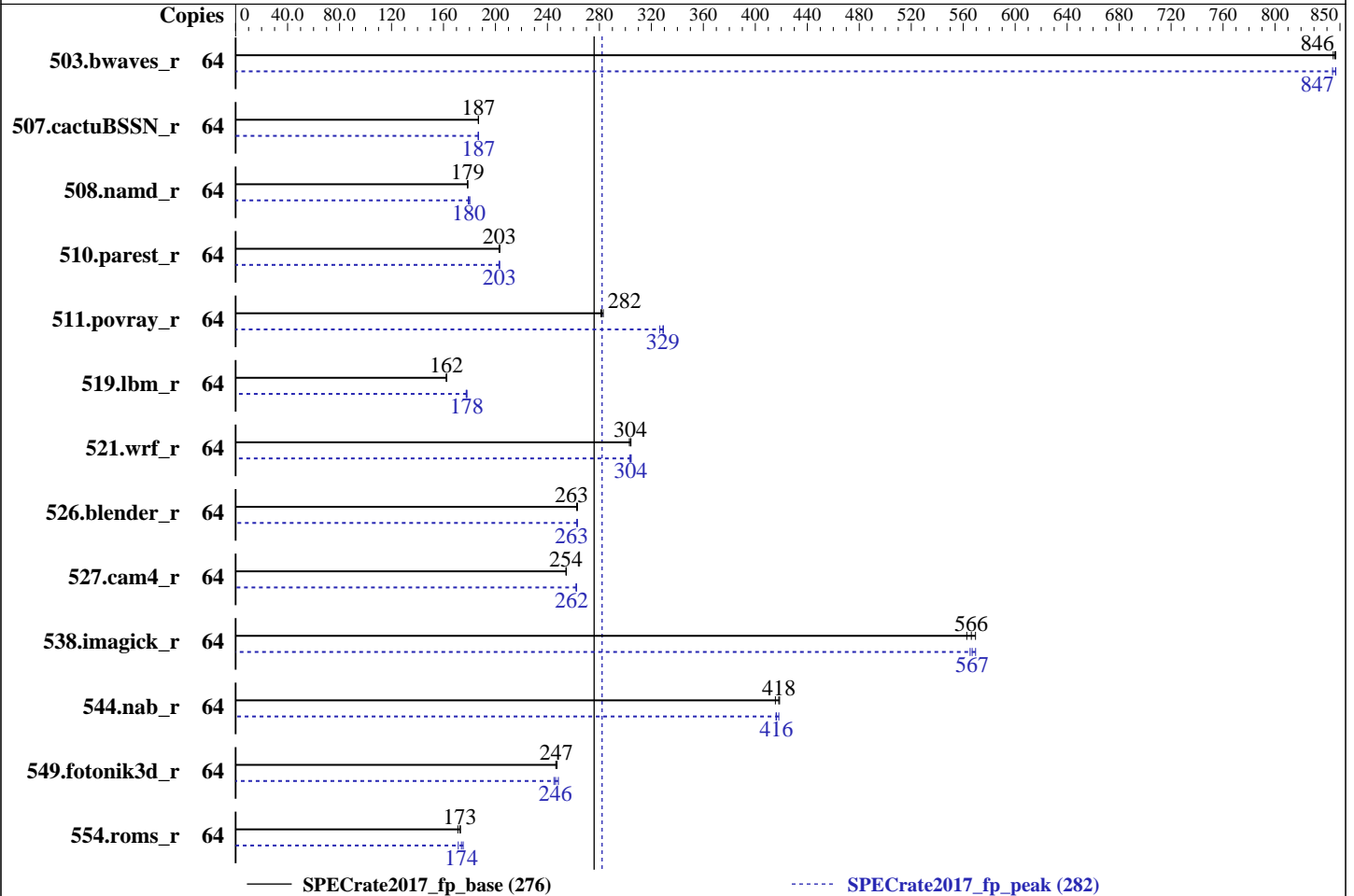
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



Hardware

CPU Name: Intel Xeon Gold 6144
 Max MHz.: 4200
 Nominal: 3500
 Enabled: 32 cores, 4 chips, 2 threads/core
 Orderable: 2,4 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 1 TB HDD, 7.2K RPM
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64 4.4.120-92.70-default)
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 3.1.3e released Jun-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: None



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	64	760	845	758	847	759	846	64	758	847	760	844	758	847
507.cactuBSSN_r	64	434	187	433	187	433	187	64	434	187	433	187	434	187
508.namd_r	64	341	179	340	179	341	178	64	337	180	340	179	339	180
510.parest_r	64	824	203	823	203	826	203	64	826	203	824	203	824	203
511.povray_r	64	528	283	530	282	532	281	64	454	329	454	329	458	327
519.lbm_r	64	415	162	416	162	416	162	64	379	178	380	177	379	178
521.wrf_r	64	472	304	471	304	473	303	64	471	304	473	303	471	304
526.blender_r	64	371	263	371	263	370	263	64	371	263	371	263	371	263
527.cam4_r	64	440	254	440	254	440	255	64	427	262	427	262	427	262
538.imagick_r	64	281	566	283	563	280	569	64	282	565	279	570	281	567
544.nab_r	64	257	419	258	418	259	415	64	259	416	259	416	258	418
549.fotonik3d_r	64	1010	247	1008	247	1012	246	64	1013	246	1004	248	1018	245
554.roms_r	64	594	171	588	173	589	173	64	593	171	581	175	585	174

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)



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General Notes (Continued)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-9r4j Mon Nov 12 01:10:47 2018

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

 model name : Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz

 4 "physical id"s (chips)

 64 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

 cpu cores : 8

 siblings : 16

 physical 0: cores 0 2 3 9 16 19 26 27

 physical 1: cores 0 2 3 9 16 19 26 27

 physical 2: cores 0 2 3 9 16 19 26 27

 physical 3: cores 0 2 3 9 16 19 26 27

From lscpu:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 64

On-line CPU(s) list: 0-63

Thread(s) per core: 2

Core(s) per socket: 8

Socket(s): 4

NUMA node(s): 8

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Platform Notes (Continued)

```

Vendor ID:           GenuineIntel
CPU family:         6
Model:              85
Model name:         Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz
Stepping:           4
CPU MHz:            4166.345
CPU max MHz:        4200.0000
CPU min MHz:        1200.0000
BogoMIPS:           6992.47
Virtualization:     VT-x
L1d cache:          32K
L1i cache:          32K
L2 cache:           1024K
L3 cache:           25344K
NUMA node0 CPU(s): 0,1,3,4,32,33,35,36
NUMA node1 CPU(s): 2,5-7,34,37-39
NUMA node2 CPU(s): 8,9,11,12,40,41,43,44
NUMA node3 CPU(s): 10,13-15,42,45-47
NUMA node4 CPU(s): 16,17,19,20,48,49,51,52
NUMA node5 CPU(s): 18,21-23,50,53-55
NUMA node6 CPU(s): 24,25,27,28,56,57,59,60
NUMA node7 CPU(s): 26,29-31,58,61-63

```

```

Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx fl16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 25344 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 8 nodes (0-7)
node 0 cpus: 0 1 3 4 32 33 35 36
node 0 size: 192094 MB
node 0 free: 191939 MB
node 1 cpus: 2 5 6 7 34 37 38 39
node 1 size: 193528 MB
node 1 free: 193221 MB
node 2 cpus: 8 9 11 12 40 41 43 44
node 2 size: 193528 MB

```

(Continued on next page)



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Platform Notes (Continued)

```

node 2 free: 193401 MB
node 3 cpus: 10 13 14 15 42 45 46 47
node 3 size: 193528 MB
node 3 free: 193383 MB
node 4 cpus: 16 17 19 20 48 49 51 52
node 4 size: 193528 MB
node 4 free: 193391 MB
node 5 cpus: 18 21 22 23 50 53 54 55
node 5 size: 193528 MB
node 5 free: 193399 MB
node 6 cpus: 24 25 27 28 56 57 59 60
node 6 size: 193528 MB
node 6 free: 193399 MB
node 7 cpus: 26 29 30 31 58 61 62 63
node 7 size: 193525 MB
node 7 free: 193380 MB
node distances:
node   0   1   2   3   4   5   6   7
  0:  10  11  21  21  21  21  21  21
  1:  11  10  21  21  21  21  21  21
  2:  21  21  10  11  21  21  21  21
  3:  21  21  11  10  21  21  21  21
  4:  21  21  21  21  10  11  21  21
  5:  21  21  21  21  11  10  21  21
  6:  21  21  21  21  21  21  10  11
  7:  21  21  21  21  21  21  11  10

```

From /proc/meminfo

```

MemTotal:      1583913440 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

From /etc/*release* /etc/*version*

SuSE-release:

```

SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2

```

```

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

```

os-release:

```

NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

```

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Platform Notes (Continued)

```

uname -a:
Linux linux-9r4j 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Oct 25 15:01

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   930G  244G  687G  27% /

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
Memory:
48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

```

Compiler Version Notes

```

=====
CC 519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base, peak)
-----

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

CC 519.lbm_r(peak)
-----

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

=====
CXXC 508.namd_r(base) 510.parest_r(base, peak)
-----

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

=====
CXXC 508.namd_r(peak)

```

(Continued on next page)



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Compiler Version Notes (Continued)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
CC 511.povray_r(base) 526.blender_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
CC 511.povray_r(peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
FC 507.cactuBSSN_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
FC 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
FC 554.roms_r(peak)

ifort (IFORT) 18.0.2 20180210
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(Continued on next page)



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Compiler Version Notes (Continued)

=====
CC 521.wrf_r(base) 527.cam4_r(base)
=====

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
CC 521.wrf_r(peak) 527.cam4_r(peak)
=====

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64

507.cactuBSSN_r: -DSPEC_LP64

(Continued on next page)



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Base Portability Flags (Continued)

```

508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

```

Base Optimization Flags

C benchmarks:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

```

C++ benchmarks:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

```

Fortran benchmarks:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

```

Benchmarks using both Fortran and C:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

```

Benchmarks using both C and C++:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

```

Benchmarks using Fortran, C, and C++:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

```

Peak Compiler Invocation

C benchmarks:

```

icc -m64 -std=c11

```

(Continued on next page)



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Peak Compiler Invocation (Continued)

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

```
538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

```
544.nab_r: Same as 538.imagick_r
```

C++ benchmarks:

```
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

```
510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

(Continued on next page)



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Peak Optimization Flags (Continued)

Fortran benchmarks:

```
503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -auto
-nostandard-realloc-lhs
```

549.fotonik3d_r: Same as 503.bwaves_r

```
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

Benchmarks using both Fortran and C:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

```
526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>



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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-11-12 01:10:46-0500.

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