



SPEC® CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp®_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019

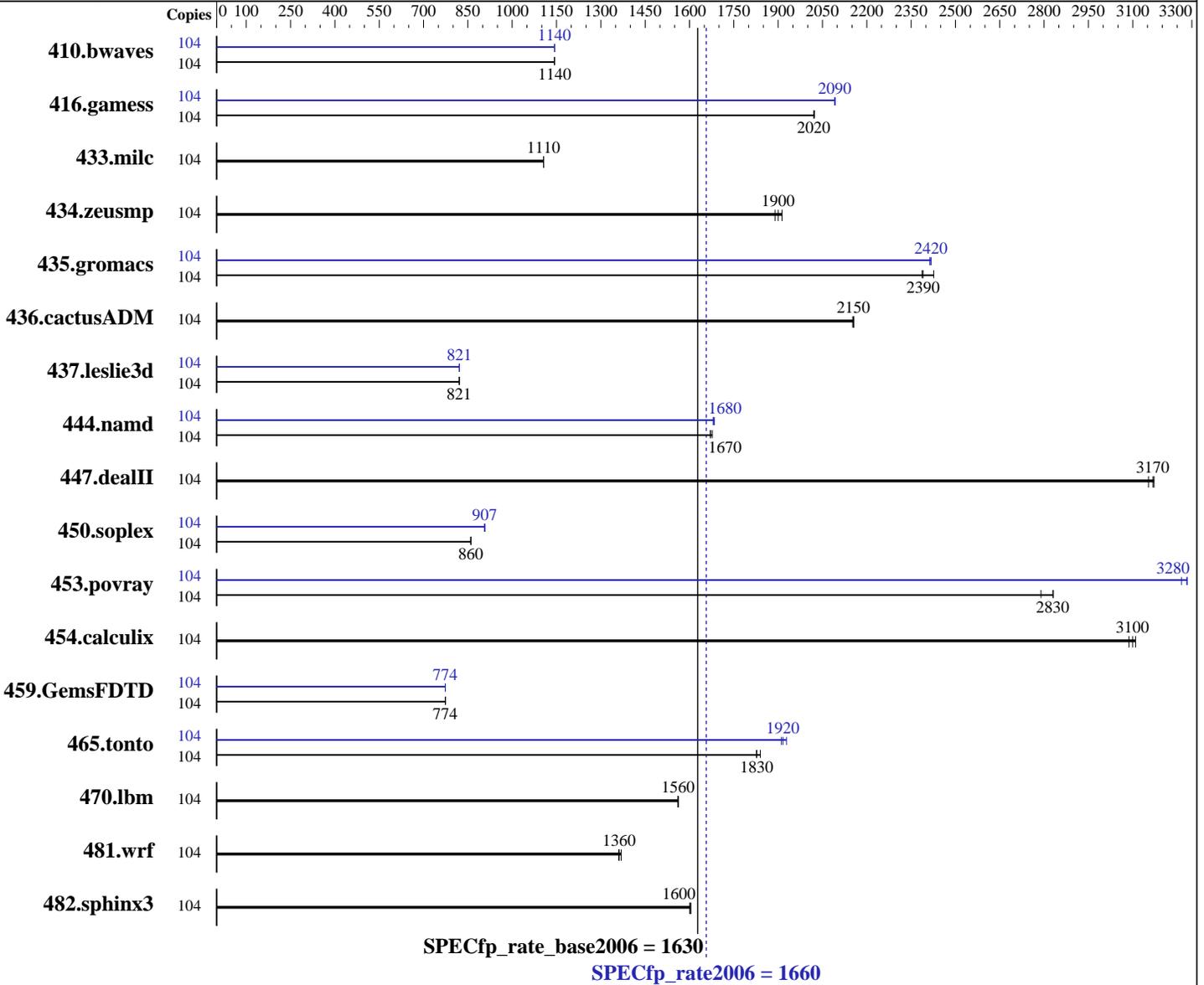
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Jun-2017



Hardware

CPU Name: Intel Xeon Platinum 8164
 CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
 CPU MHz: 2000
 FPU: Integrated
 CPU(s) enabled: 52 cores, 2 chips, 26 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 1 MB I+D on chip per core

Continued on next page

Software

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
 Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
 Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
 Auto Parallel: Yes
 File System: xfs
 System State: Run level 3 (multi-user)

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Jun-2017

L3 Cache: 35.75 MB I+D on chip per chip
Other Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 600 GB SAS HDD, 10K RPM
Other Hardware: None

Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: None

Results Table

| Benchmark | Base | | | | | | | Peak | | | | | | |
|---------------|--------|-------------|-------------|-------------|-------------|-------------|-------------|--------|-------------|-------------|------------|-------------|-------------|-------------|
| | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 410.bwaves | 104 | <u>1236</u> | <u>1140</u> | 1236 | 1140 | 1237 | 1140 | 104 | 1236 | 1140 | 1237 | 1140 | <u>1236</u> | <u>1140</u> |
| 416.gamess | 104 | 1008 | 2020 | <u>1008</u> | <u>2020</u> | 1007 | 2020 | 104 | 973 | 2090 | <u>973</u> | <u>2090</u> | 974 | 2090 |
| 433.milc | 104 | <u>863</u> | <u>1110</u> | 863 | 1110 | 863 | 1110 | 104 | <u>863</u> | <u>1110</u> | 863 | 1110 | 863 | 1110 |
| 434.zeusmp | 104 | <u>498</u> | <u>1900</u> | 495 | 1910 | 501 | 1890 | 104 | <u>498</u> | <u>1900</u> | 495 | 1910 | 501 | 1890 |
| 435.gromacs | 104 | <u>311</u> | <u>2390</u> | 311 | 2390 | 306 | 2430 | 104 | 308 | 2410 | 307 | 2420 | <u>307</u> | <u>2420</u> |
| 436.cactusADM | 104 | 577 | 2150 | 576 | 2160 | <u>577</u> | <u>2150</u> | 104 | 577 | 2150 | 576 | 2160 | <u>577</u> | <u>2150</u> |
| 437.leslie3d | 104 | 1192 | 820 | 1189 | 822 | <u>1191</u> | <u>821</u> | 104 | 1191 | 821 | 1190 | 822 | <u>1191</u> | <u>821</u> |
| 444.namd | 104 | 497 | 1680 | <u>499</u> | <u>1670</u> | 499 | 1670 | 104 | 496 | 1680 | 495 | 1680 | <u>496</u> | <u>1680</u> |
| 447.dealII | 104 | 377 | 3150 | 375 | 3170 | <u>376</u> | <u>3170</u> | 104 | 377 | 3150 | 375 | 3170 | <u>376</u> | <u>3170</u> |
| 450.soplex | 104 | <u>1008</u> | <u>860</u> | 1009 | 860 | 1008 | 860 | 104 | <u>957</u> | <u>907</u> | 957 | 906 | 956 | 908 |
| 453.povray | 104 | <u>196</u> | <u>2830</u> | 198 | 2790 | 195 | 2830 | 104 | 168 | 3280 | <u>169</u> | <u>3280</u> | 169 | 3270 |
| 454.calculix | 104 | 278 | 3090 | <u>277</u> | <u>3100</u> | 276 | 3110 | 104 | 278 | 3090 | <u>277</u> | <u>3100</u> | 276 | 3110 |
| 459.GemsFDTD | 104 | 1425 | 774 | 1427 | 773 | <u>1426</u> | <u>774</u> | 104 | <u>1426</u> | <u>774</u> | 1426 | 774 | 1426 | 774 |
| 465.tonto | 104 | 556 | 1840 | 560 | 1830 | <u>560</u> | <u>1830</u> | 104 | <u>534</u> | <u>1920</u> | 531 | 1930 | 536 | 1910 |
| 470.lbm | 104 | <u>915</u> | <u>1560</u> | 915 | 1560 | 916 | 1560 | 104 | <u>915</u> | <u>1560</u> | 915 | 1560 | 916 | 1560 |
| 481.wrf | 104 | 854 | 1360 | 849 | 1370 | <u>853</u> | <u>1360</u> | 104 | 854 | 1360 | 849 | 1370 | <u>853</u> | <u>1360</u> |
| 482.sphinx3 | 104 | 1266 | 1600 | 1263 | 1600 | <u>1264</u> | <u>1600</u> | 104 | 1266 | 1600 | 1263 | 1600 | <u>1264</u> | <u>1600</u> |

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-j64x Fri Dec 15 05:10:36 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: <http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
 2 "physical id"s (chips)
 104 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
  cpu cores : 26
  siblings  : 52
  physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25
 26 27 28 29
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25
 26 27 28 29
cache size : 36608 KB
```

```
From /proc/meminfo
MemTotal:      394864040 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2
```

```
From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or
release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017

Platform Notes (Continued)

```
uname -a:
Linux linux-j64x 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 14 02:28
```

```
SPEC is set to: /home/cpu2006-1.2
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdc7        xfs   416G  97G  320G  24% /home
Additional information from dmidecode:
```

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017

Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, <http://www.spec.org/osg/policy.html>

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017

General Notes (Continued)

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
-qopt-mem-layout-trans=3

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Jun-2017

Base Optimization Flags (Continued)

C++ benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
-qopt-mem-layout-trans=3

Fortran benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Benchmarks using both Fortran and C:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
-qopt-mem-layout-trans=3

Peak Compiler Invocation

C benchmarks:

icc -m64

C++ benchmarks (except as noted below):

icpc -m64

450.soplex: icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

icc -m64 ifort -m64

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.deallI: -DSPEC_CPU_LP64
450.soplex: -D_FILE_OFFSET_BITS=64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Jun-2017

Peak Portability Flags (Continued)

482.sphinx3: -DSPEC_CPU_LP64

Peak Optimization Flags

C benchmarks:

433.milc: basepeak = yes

470.lbm: basepeak = yes

482.sphinx3: basepeak = yes

C++ benchmarks:

444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -fno-alias -auto-ilp32
-qopt-mem-layout-trans=3

447.dealII: basepeak = yes

450.soplex: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-malloc-options=3
-qopt-mem-layout-trans=3

453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -qopt-mem-layout-trans=3

Fortran benchmarks:

410.bwaves: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-

434.zeusmp: basepeak = yes

437.leslie3d: Same as 410.bwaves

459.GemsFDTD: Same as 410.bwaves

465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -auto -inline-calloc
-qopt-malloc-options=3

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECfp_rate2006 = 1660

SPECfp_rate_base2006 = 1630

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Jun-2017

Peak Optimization Flags (Continued)

Benchmarks using both Fortran and C:

435.gromacs: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -qopt-prefetch -auto-ilp32
-qopt-mem-layout-trans=3

436.cactusADM: basepeak = yes

454.calculix: basepeak = yes

481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Mon Feb 26 10:21:42 2018 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 23 February 2018.