



SPEC® CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint®2006 = 72.1

SPECint_base2006 = 70.3

CPU2006 license: 9019

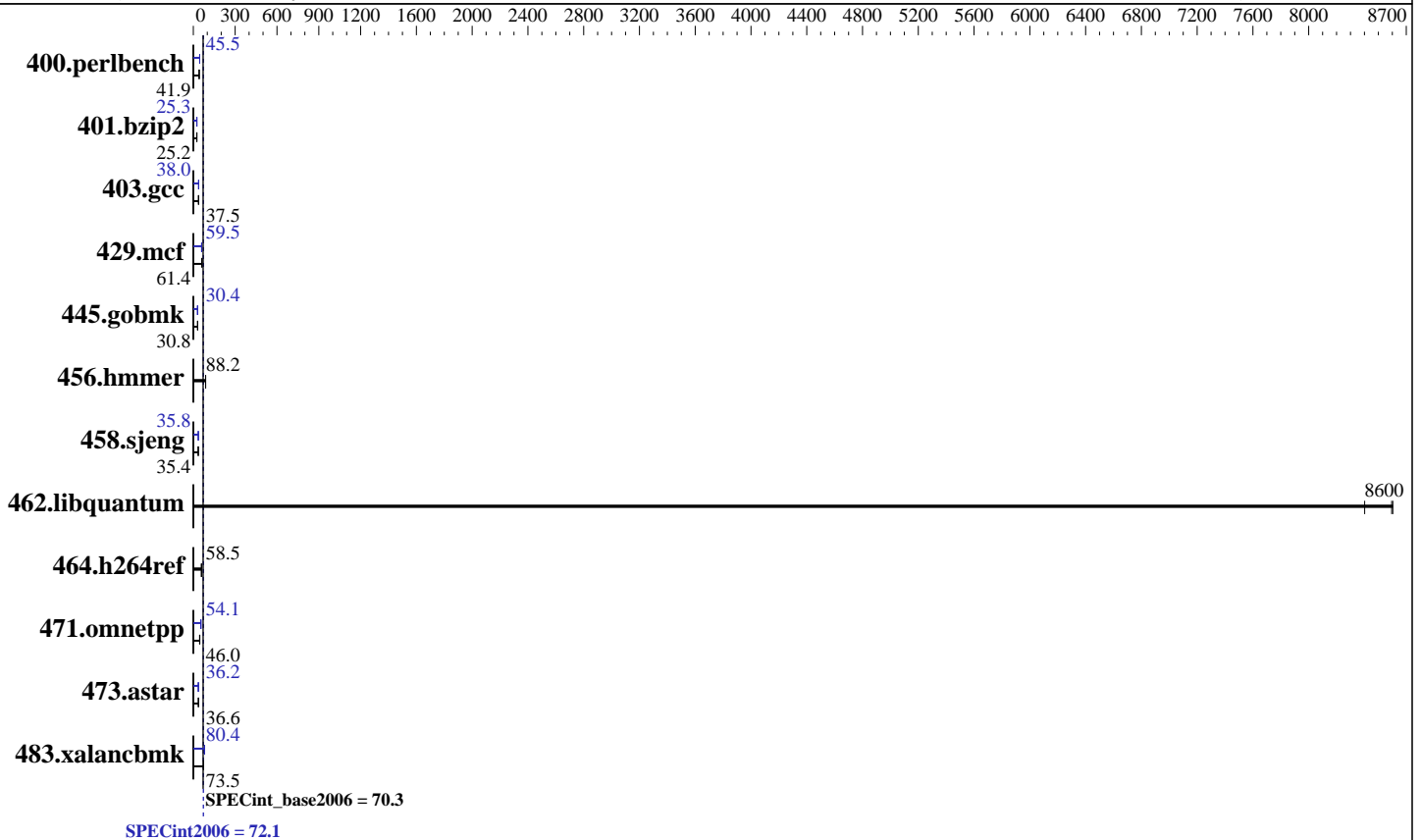
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Apr-2016

Hardware Availability: Apr-2016

Software Availability: Dec-2015



Hardware

CPU Name: Intel Xeon E5-2697 v4
 CPU Characteristics: Intel Turbo Boost Technology up to 3.60 GHz
 CPU MHz: 2300
 FPU: Integrated
 CPU(s) enabled: 36 cores, 2 chips, 18 cores/chip
 CPU(s) orderable: 1,2 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 45 MB I+D on chip per chip
 Other Cache: None
 Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2400T-R)
 Disk Subsystem: 1 x 400 GB SSD SAS
 Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 12 SP1 (x86_64) 3.12.49-11-default
 Compiler: C/C++; Version 16.0.0.101 of Intel C++ Studio XE for Linux
 Auto Parallel: Yes
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 32/64-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V10.2



SPEC CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint2006 = **72.1**

SPECint_base2006 = **70.3**

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2016
Hardware Availability: Apr-2016
Software Availability: Dec-2015

Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	234	41.8	233	41.9	<u>233</u>	<u>41.9</u>	<u>215</u>	<u>45.5</u>	215	45.5	214	45.6
401.bzip2	383	25.2	383	25.2	<u>383</u>	<u>25.2</u>	382	25.3	382	25.3	<u>382</u>	<u>25.3</u>
403.gcc	215	37.5	215	37.5	<u>215</u>	<u>37.5</u>	211	38.2	<u>212</u>	<u>38.0</u>	213	37.9
429.mcf	148	61.5	149	61.2	<u>148</u>	<u>61.4</u>	153	59.6	<u>153</u>	<u>59.5</u>	153	59.5
445.gobmk	340	30.8	341	30.7	<u>341</u>	<u>30.8</u>	<u>345</u>	<u>30.4</u>	345	30.4	345	30.4
456.hammer	106	88.3	106	88.1	<u>106</u>	<u>88.2</u>	106	88.3	106	88.1	<u>106</u>	<u>88.2</u>
458.sjeng	342	35.3	<u>342</u>	<u>35.4</u>	342	35.4	338	35.8	<u>338</u>	<u>35.8</u>	338	35.8
462.libquantum	<u>2.41</u>	<u>8600</u>	2.47	8400	2.41	8600	<u>2.41</u>	<u>8600</u>	2.47	8400	2.41	8600
464.h264ref	378	58.5	378	58.5	<u>378</u>	<u>58.5</u>	378	58.5	378	58.5	<u>378</u>	<u>58.5</u>
471.omnetpp	140	44.7	<u>136</u>	<u>46.0</u>	134	46.5	117	53.5	<u>116</u>	<u>54.1</u>	114	54.9
473.astar	<u>192</u>	<u>36.6</u>	191	36.7	193	36.4	<u>194</u>	<u>36.2</u>	196	35.8	194	36.2
483.xalancbmk	94.8	72.8	<u>93.9</u>	<u>73.5</u>	93.6	73.7	<u>85.8</u>	<u>80.4</u>	85.9	80.4	85.4	80.8

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

```

Intel Hyper-Threading Technology option set to Disabled
CPU performance set to Enterprise
Power Technology set to Energy Efficient
Energy Performance BIAS setting set to Balanced Performance
Memory RAS configuration set to Maximum Performance
Memory Power Saving Mode set to Disabled
QPI Snoop Mode set to Home Directory Snoop with OSB
Sysinfo program /opt/CISCO_Benchmarks/cpu2006/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on linux-nsg9 Wed Mar 30 00:51:17 2016

```

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: <http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2697 v4 @ 2.30GHz
2 "physical id"s (chips)

```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint2006 = 72.1

SPECint_base2006 = 70.3

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Apr-2016

Hardware Availability: Apr-2016

Software Availability: Dec-2015

Platform Notes (Continued)

36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 18
siblings  : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
cache size : 46080 KB
```

From /proc/meminfo

```
MemTotal:      264367020 kB
HugePages_Total: 0
Hugepagesize:  2048 kB
```

/usr/bin/lsb_release -d

```
SUSE Linux Enterprise Server 12 SP1
```

From /etc/*release* /etc/*version*

SuSE-release:

```
SUSE Linux Enterprise Server 12 (x86_64)
```

```
VERSION = 12
```

```
PATCHLEVEL = 1
```

```
# This file is deprecated and will be removed in a future service pack or release.
```

```
# Please check /etc/os-release for details about this release.
```

os-release:

```
NAME="SLES"
```

```
VERSION="12-SP1"
```

```
VERSION_ID="12.1"
```

```
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP1"
```

```
ID="sles"
```

```
ANSI_COLOR="0;32"
```

```
CPE_NAME="cpe:/o:suse:sles:12:sp1"
```

uname -a:

```
Linux linux-nsg9 3.12.49-11-default #1 SMP Wed Nov 11 20:52:43 UTC 2015
(8d714a0) x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Mar 29 23:35

SPEC is set to: /opt/CISCO_Benchmarks/cpu2006

```
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        xfs   325G  13G  313G  4% /
```

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M4.3.1.1.11.110420151758 11/04/2015

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint2006 = 72.1

SPECint_base2006 = 70.3

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2016
Hardware Availability: Apr-2016
Software Availability: Dec-2015

Platform Notes (Continued)

Memory:
16x 0xCE00 M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

KMP_AFFINITY = "granularity=fine,compact"

LD_LIBRARY_PATH = "/opt/CISCO_Benchmarks/cpu2006/libs/32:/opt/CISCO_Benchmarks/cpu2006/libs/64:/opt/CISCO_Benchmarks/cpu2006/sh"

OMP_NUM_THREADS = "36"

Binaries compiled on a system with 1x Intel Core i5-4670K CPU + 32GB memory using RedHat EL 7.1

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint2006 = 72.1

SPECint_base2006 = 70.3

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Apr-2016

Hardware Availability: Apr-2016

Software Availability: Dec-2015

Base Optimization Flags (Continued)

C++ benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh -lsmartheap64

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m64

400.perlbench: icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):

icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32

401.bzip2: -DSPEC_CPU_LP64

403.gcc: -DSPEC_CPU_LP64

429.mcf: -DSPEC_CPU_LP64

445.gobmk: -D_FILE_OFFSET_BITS=64

456.hmmer: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

464.h264ref: -DSPEC_CPU_LP64

471.omnetpp: -D_FILE_OFFSET_BITS=64

473.astar: -DSPEC_CPU_LP64

483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX



SPEC CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint2006 = 72.1

SPECint_base2006 = 70.3

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Apr-2016

Hardware Availability: Apr-2016

Software Availability: Dec-2015

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -opt-prefetch
-ansi-alias

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div
-par-num-threads=1(pass 1) -prof-use(pass 2) -auto-ilp32
-opt-prefetch -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
-opt-malloc-options=3 -auto-ilp32

429.mcf: -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
-opt-prefetch -auto-p32

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-prof-use(pass 2) -par-num-threads=1(pass 1) -ansi-alias

456.hmmer: basepeak = yes

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -unroll4

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2)
-opt-ra-region-strategy=block -ansi-alias
-Wl,-z,muldefs -L/sh -lsmartheap

473.astar: -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-auto-p32 -Wl,-z,muldefs -L/sh -lsmartheap64

483.xalancbmk: -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-ansi-alias -Wl,-z,muldefs -L/sh -lsmartheap



SPEC CINT2006 Result

Copyright 2006-2016 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2697 v4, 2.30 GHz)

SPECint2006 = 72.1

SPECint_base2006 = 70.3

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Apr-2016

Hardware Availability: Apr-2016

Software Availability: Dec-2015

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revD.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revD.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Tue May 3 18:01:36 2016 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 3 May 2016.