# SPEC CPU®2017 Integer Speed Result

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6244, 3.60GHz)

| SPECspeed®2017_int_base = 11.1 |
| SPECspeed®2017_int_peak = Not Run |

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Mar-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** Nov-2018

### Threads

<table>
<thead>
<tr>
<th>Specbench</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base (11.1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>7.59</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>10.9</td>
</tr>
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</tr>
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</tr>
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<td>32</td>
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</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>15.4</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>5.98</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>5.39</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>15.9</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>32</td>
<td>25.6</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6244  
- **Max MHz:** 4400  
- **Nominal:** 3600  
- **Enabled:** 32 cores, 4 chips  
- **Orderable:** 2,4 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **Cache L2:** 1 MB I+D on chip per core  
- **Cache L3:** 24.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 300 GB 10K RPM SAS HDD  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.3.32 released Mar-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** --
SPEC CPU®2017 Integer Speed Result

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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>234</td>
<td>7.59</td>
<td>234</td>
<td>7.59</td>
<td>234</td>
<td>7.58</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>366</td>
<td>10.9</td>
<td>366</td>
<td>10.9</td>
<td>367</td>
<td>10.9</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>341</td>
<td>13.8</td>
<td>341</td>
<td>13.8</td>
<td>341</td>
<td>13.8</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>32</td>
<td>190</td>
<td>8.61</td>
<td>194</td>
<td>8.43</td>
<td>190</td>
<td>8.59</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>32</td>
<td>102</td>
<td>13.9</td>
<td>102</td>
<td>13.9</td>
<td>101</td>
<td>14.0</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>115</td>
<td>15.4</td>
<td>115</td>
<td>15.4</td>
<td>117</td>
<td>15.1</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>240</td>
<td>5.98</td>
<td>240</td>
<td>5.98</td>
<td>240</td>
<td>5.98</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>316</td>
<td>5.39</td>
<td>317</td>
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<td>15.9</td>
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</tr>
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<td>32</td>
<td>242</td>
<td>25.6</td>
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<td>25.6</td>
<td>241</td>
<td>25.6</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using RedHat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
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Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-lozz Mon Mar 18 15:23:14 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
 4 "physical id"s (chips)
32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 3 9 17 18 24 25 27
physical 1: cores 1 4 9 11 17 18 25 27
physical 2: cores 1 2 9 17 19 20 26 27
physical 3: cores 2 8 9 18 19 20 25 26

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
Stepping: 6
CPU MHz: 3600.000
CPU max MHz: 4400.0000
CPU min MHz: 1200.0000
BogoMIPS: 7200.00
Virtualization: VT-x

(Continued on next page)
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Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
NUMA node2 CPU(s): 16-23
NUMA node3 CPU(s): 24-31
Flags: fpu vme de pse tsc msr pae mce cmov cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpref perf_counter tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single mtrr pabs cmov nonstop_tsc tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mxs rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt axv512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occp_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pni pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 386572 MB
  node 0 free: 386226 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 387059 MB
  node 1 free: 386893 MB
  node 2 cpus: 16 17 18 19 20 21 22 23
  node 2 size: 387030 MB
  node 2 free: 386812 MB
  node 3 cpus: 24 25 26 27 28 29 30 31
  node 3 size: 387057 MB
  node 3 free: 386621 MB
  node distances:
    node 0 1 2 3
    0: 10 21 21 21
    1: 21 10 21 21
    2: 21 21 10 21
    3: 21 21 21 10

From /proc/meminfo

(Continued on next page)
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Platform Notes (Continued)

MemTotal: 1584866252 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
o-release:
   NAME="SLES"
   VERSION="15"
   VERSION_ID="15"
   PRETTY_NAME="SUSE Linux Enterprise Server 15"
   ID="sles"
   ID_LIKE="suse"
   ANSI_COLOR="0;32"
   CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-lozz 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Mar 18 14:19

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 273G 33G 241G 12% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C    | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
==============================================================================

(Continued on next page)
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**Compiler Version Notes (Continued)**

<table>
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<tr>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
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</thead>
<tbody>
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<td></td>
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**Base Compiler Invocation**

**C benchmarks:**
icc -m64 -std=c11

**C++ benchmarks:**
icpc -m64

**Fortran benchmarks:**
ifort -m64

**Base Portability Flags**

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64
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Base Portability Flags (Continued)

631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
- L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
- lqkmalloc

Fortran benchmarks:
- xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
- nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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