



# SPEC® CPU2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4114  
2.20 GHz)

SPECspeed2017\_int\_base = 7.17

SPECspeed2017\_int\_peak = 7.35

CPU2017 License: 9019

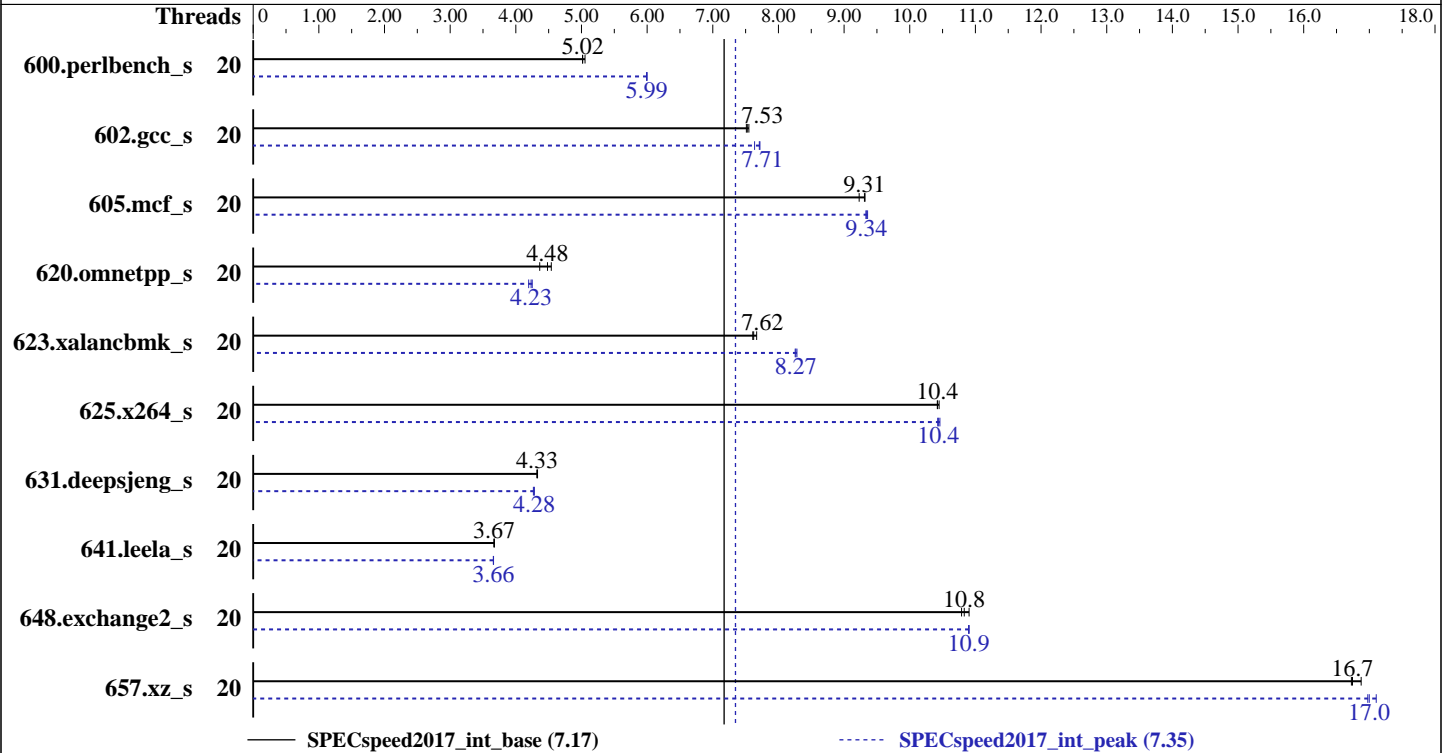
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2018

Hardware Availability: Aug-2017

Software Availability: Oct-2018



### Hardware

CPU Name: Intel Xeon Silver 4114  
 Max MHz.: 3000  
 Nominal: 2200  
 Enabled: 20 cores, 2 chips  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 13.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)  
 Storage: 1 x 400 GB SAS SSD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.120-92.70-default  
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 4.0.1 released Oct-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1



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## Results Table

Benchmark	Base						Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	20	<b>354</b>	<b>5.02</b>	351	5.05	354	5.02	20	296	5.99	<b>296</b>	<b>5.99</b>	296	6.00
602.gcc_s	20	530	7.51	527	7.55	<b>529</b>	<b>7.53</b>	20	516	7.72	521	7.64	<b>517</b>	<b>7.71</b>
605.mcf_s	20	512	9.23	<b>507</b>	<b>9.31</b>	507	9.32	20	<b>505</b>	<b>9.34</b>	506	9.33	505	9.36
620.omnetpp_s	20	<b>364</b>	<b>4.48</b>	374	4.36	359	4.54	20	389	4.20	<b>385</b>	<b>4.23</b>	384	4.25
623.xalancbmk_s	20	186	7.61	185	7.67	<b>186</b>	<b>7.62</b>	20	172	8.26	171	8.28	<b>171</b>	<b>8.27</b>
625.x264_s	20	<b>169</b>	<b>10.4</b>	169	10.4	169	10.4	20	169	10.4	<b>169</b>	<b>10.4</b>	169	10.5
631.deepsjeng_s	20	331	4.33	<b>331</b>	<b>4.33</b>	332	4.32	20	335	4.28	336	4.27	<b>335</b>	<b>4.28</b>
641.leela_s	20	464	3.67	<b>465</b>	<b>3.67</b>	465	3.67	20	466	3.66	466	3.66	<b>466</b>	<b>3.66</b>
648.exchange2_s	20	270	10.9	272	10.8	<b>271</b>	<b>10.8</b>	20	270	10.9	<b>270</b>	<b>10.9</b>	270	10.9
657.xz_s	20	370	16.7	<b>369</b>	<b>16.7</b>	366	16.9	20	<b>364</b>	<b>17.0</b>	361	17.1	364	17.0

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

KMP\_AFFINITY = "granularity=fine,scatter"

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



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## Platform Notes

### BIOS Settings:

Intel HyperThreading Technology set to Disabled  
 CPU performance set to Enterprise  
 Power Performance Tuning set to OS Controls  
 SNC set to Disabled  
 Patrol Scrub set to Disabled  
 Sysinfo program /home/cpu2017/bin/sysinfo  
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
 running on linux-dkz7 Wed Dec 12 11:08:28 2018

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

### From /proc/cpuinfo

```

model name      : Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
 2 "physical id"s (chips)
 20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 10
siblings       : 10
physical 0:    : cores 0 1 2 3 4 8 9 10 11 12
physical 1:    : cores 0 1 2 3 4 8 9 10 11 12

```

### From lscpu:

```

Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          20
On-line CPU(s) list:  0-19
Thread(s) per core:  1
Core(s) per socket:  10
Socket(s):       2
NUMA node(s):    2
Vendor ID:       GenuineIntel
CPU family:      6
Model:           85
Model name:      Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
Stepping:        4
CPU MHz:         2093.273
CPU max MHz:     3000.0000
CPU min MHz:     800.0000
BogoMIPS:        4389.66
Virtualization:  VT-x
L1d cache:       32K
L1i cache:       32K

```

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### Platform Notes (Continued)

L2 cache: 1024K  
L3 cache: 14080K  
NUMA node0 CPU(s): 0-9  
NUMA node1 CPU(s): 10-19

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov  
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp  
lm constant\_tsc art arch\_perfmon pebs bts rep\_good nopl xtopology nonstop\_tsc  
aperfperf eagerfpu pni pclmulqdq dtes64 monitor ds\_cpl vmx smx est tm2 ssse3 sdbg  
fma cx16 xtpr pdcm pcid dca sse4\_1 sse4\_2 x2apic movbe popcnt tsc\_deadline\_timer aes  
xsave avx f16c rdrand lahf\_lm abm 3dnowprefetch ida arat epb invpcid\_single pln pts  
dtherm hwp hwp\_act\_window hwp\_epp hwp\_pkg\_req intel\_pt rsb\_ctxsw spec\_ctrl stibp  
retpoline kaiser tpr\_shadow vnmi flexpriority ept vpid fsgsbase tsc\_adjust bmi1 hle  
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt  
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm\_llc cqm\_occup\_llc

```
/proc/cpuinfo cache data
cache size : 14080 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9
node 0 size: 385626 MB
node 0 free: 385101 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19
node 1 size: 387054 MB
node 1 free: 386606 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal: 791225612 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
```

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## Platform Notes (Continued)

```
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 12 11:06
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda2        xfs   500G  118G  383G   24% /
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:  
12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400  
12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

## Compiler Version Notes

```
=====  
CC 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base,  
peak) 657.xz_s(base)  
-----
```

```
icc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----
```

```
=====  
CC 600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)  
-----
```

```
icc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----
```

```
=====  
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
-----
```

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### Compiler Version Notes (Continued)

641.leela\_s(base)

-----  
icpc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
CXXC 620.omnetpp\_s(peak) 623.xalancbmk\_s(peak) 631.deepsjeng\_s(peak)  
641.leela\_s(peak)  
-----

icpc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
FC 648.exchange2\_s(base, peak)  
-----

ifort (IFORT) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

### Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

C++ benchmarks:  
icpc -m64

Fortran benchmarks:  
ifort -m64

### Base Portability Flags

600.perlbench\_s: -DSPEC\_LP64 -DSPEC\_LINUX\_X64  
602.gcc\_s: -DSPEC\_LP64  
605.mcf\_s: -DSPEC\_LP64  
620.omnetpp\_s: -DSPEC\_LP64  
623.xalancbmk\_s: -DSPEC\_LP64 -DSPEC\_LINUX  
625.x264\_s: -DSPEC\_LP64  
631.deepsjeng\_s: -DSPEC\_LP64  
641.leela\_s: -DSPEC\_LP64  
648.exchange2\_s: -DSPEC\_LP64

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## Base Portability Flags (Continued)

657.xz\_s: -DSPEC\_LP64

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
623.xalancbmk_s: icpc -m32 -L/opt/intel/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64
```

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## Peak Portability Flags (Continued)

631.deepsjeng\_s: -DSPEC\_LP64  
641.leela\_s: -DSPEC\_LP64  
648.exchange2\_s: -DSPEC\_LP64  
657.xz\_s: -DSPEC\_LP64

## Peak Optimization Flags

C benchmarks:

600.perlbench\_s: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC\_SUPPRESS\_OPENMP -qopenmp  
-DSPEC\_OPENMP -fno-strict-overflow  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

602.gcc\_s: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC\_SUPPRESS\_OPENMP -qopenmp  
-DSPEC\_OPENMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

605.mcf\_s: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

625.x264\_s: -w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

657.xz\_s: Same as 602.gcc\_s

C++ benchmarks:

620.omnetpp\_s: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

623.xalancbmk\_s: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

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## Peak Optimization Flags (Continued)

631.deepsjeng\_s: Same as 620.omnetpp\_s

641.leela\_s: Same as 620.omnetpp\_s

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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