SPEC® CINT2006 Result

IBM Corporation

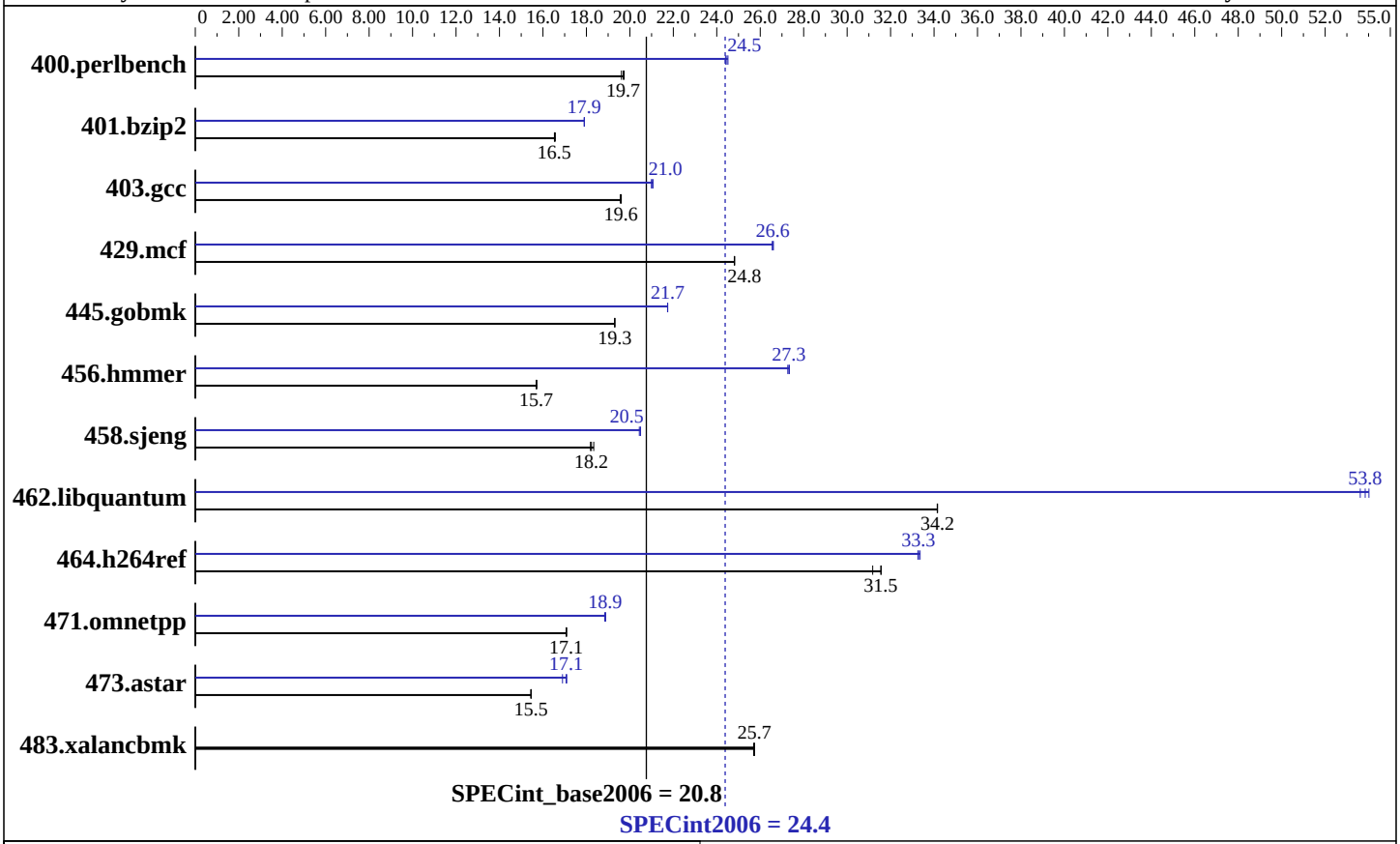
IBM BladeCenter HS12 (Intel Xeon E3113)

SPECint®2006 = 24.4

SPECint_base2006 = 20.8

CPU2006 license: 11
Test sponsor: IBM Corporation
Tested by: IBM Corporation

Test date: Apr-2008
Hardware Availability: Jun-2008
Software Availability: Nov-2007



Hardware

CPU Name:	Intel Xeon E3113
CPU Characteristics:	1333MHz system bus
CPU MHz:	3000
FPU:	Integrated
CPU(s) enabled:	2 cores, 1 chip, 2 cores/chip
CPU(s) orderable:	1 chip
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	6 MB I+D on chip per chip
L3 Cache:	None
Other Cache:	None
Memory:	8 GB (4 x 2 GB DDR2-5300 ECC)
Disk Subsystem:	1 x 73 GB SAS, 10000 RPM
Other Hardware:	None

Software

Operating System:	SuSE Linux Enterprise Server 10 (x86_64) SP1, Kernel 2.6.16.46-0.12-smp
Compiler:	Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
Auto Parallel:	Yes
File System:	ReiserFS
System State:	Multi-user, run level 3
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15

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Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	**496**	**19.7**	498	19.6	495	19.7	399	24.5	400	24.4	**399**	**24.5**
401.bzip2	582	16.6	**584**	**16.5**	584	16.5	539	17.9	539	17.9	**539**	**17.9**
403.gcc	412	19.6	**411**	**19.6**	411	19.6	384	21.0	382	21.1	**383**	**21.0**
429.mcf	368	24.8	**367**	**24.8**	367	24.8	343	26.6	**343**	**26.6**	343	26.6
445.gobmk	543	19.3	543	19.3	**543**	**19.3**	**483**	**21.7**	482	21.7	483	21.7
456.hmmer	593	15.7	595	15.7	**594**	**15.7**	**342**	**27.3**	342	27.3	341	27.3
458.sjeng	**664**	**18.2**	665	18.2	660	18.3	**591**	**20.5**	590	20.5	592	20.4
462.libquantum	607	34.2	607	34.1	**607**	**34.2**	384	54.0	386	53.6	**385**	**53.8**
464.h264ref	710	31.2	701	31.6	**701**	**31.5**	663	33.4	665	33.3	**665**	**33.3**
471.omnetpp	366	17.1	**366**	**17.1**	366	17.1	331	18.9	**331**	**18.9**	332	18.8
473.astar	454	15.5	455	15.4	**454**	**15.5**	**411**	**17.1**	411	17.1	415	16.9
483.xalancbmk	**268**	**25.7**	268	25.7	269	25.7	**268**	**25.7**	268	25.7	269	25.7

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

```
All benchmarks compiled in 32-bit mode except 401.bzip2 and 456.hmmer,
for peak, are compiled in 64-bit mode
Hardware Sector Prefetch Enabled and Adjacent Sector Prefetch Enabled
OMP_NUM_THREADS set to number of cores
KMP_AFFINITY set to physical,0
KMP_STACKSIZE set to null
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Base Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Base Optimization Flags

C benchmarks:
```
-fast -vec-guard-write -parallel -par-runtime-control
```

C++ benchmarks:
```
-xT -ipo -O3 -no-prec-div -Wl,-z,muldefs
-L/spec/users/rahul/cpu2006.1.0/lib  -lsmartheap
```

Base Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc
```

401.bzip2:
```
/opt/intel/cce/10.1.008/bin/icc
-L/opt/intel/cce/10.1.008/lib
-I/opt/intel/cce/10.1.008/include
```

456.hmmer:
```
/opt/intel/cce/10.1.008/bin/icc
-L/opt/intel/cce/10.1.008/lib
-I/opt/intel/cce/10.1.008/include
```

C++ benchmarks:
```
icpc
```

Peak Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
401.bzip2: `-DSPEC_CPU_LP64`
456.hmmer: `-DSPEC_CPU_LP64`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Peak Optimization Flags

C benchmarks:

Continued on next page

Peak Optimization Flags (Continued)

400.perlbench: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-fast -ansi-alias -prefetch`

401.bzip2: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-fast -prefetch -auto-ilp32`

403.gcc: `-fast -inline-calloc -opt-malloc-options=3`

429.mcf: `-fast -prefetch`

445.gobmk: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xT -O2 -ipo -no-prec-div -ansi-alias`

456.hmmer: `-fast -unroll2 -ansi-alias -opt-multi-version-aggressive -auto-ilp32`

458.sjeng: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-fast -unroll4`

462.libquantum: `-fast -unroll4 -Ob0 -prefetch -opt-streaming-stores always -vec-guard-write -opt-malloc-options=3 -parallel -par-runtime-control`

464.h264ref: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-fast -unroll2 -ansi-alias`

C++ benchmarks:

471.omnetpp: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xT -O3 -ipo -no-prec-div -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap`

473.astar: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xT -O3 -ipo -no-prec-div -ansi-alias -opt-ra-region-strategy=routine -Wl,-z,muldefs -L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap`

483.xalancbmk: `basepeak = yes`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic10.1-int-linux64-revC.20090714.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic10.1-int-linux64-revC.20090714.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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