SPEC CPU®2017 Integer Speed Result

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SDI100A2R-22
(2.60 GHz, Intel Xeon Gold 6348)

$SPECspeed®2017\_int\_base = 11.9$

$SPECspeed®2017\_int\_peak = 12.2$

CPU2017 License: 006042　　　　　　　　　　　　　　　　**Test Date:**　　　Jul-2021
Test Sponsor:　Netweb Pte Ltd　　　　　　　　　　　　**Hardware Availability:** Apr-2021
Tested by:　　　Tyrone Systems　　　　　　　　　　　　**Software Availability:**　Jun-2021

Threads	
600.perlbench_s 112	7.21 / 8.31
602.gcc_s 112	10.9 / 11.5
605.mcf_s 112	19.9
620.omnetpp_s 112	11.7
623.xalancbmk_s 112	13.6
625.x264_s 112	17.1 / 17.9
631.deepsjeng_s 112	5.93
641.leela_s 112	4.86
648.exchange2_s 112	19.1
657.xz_s 112	24.3

SPECspeed®2017_int_base (11.9)　　　　　SPECspeed®2017_int_peak (12.2)

Hardware

CPU Name: Intel Xeon Gold 6348
　Max MHz: 3500
　Nominal:　2600
Enabled:　56 cores, 2 chips, 2 threads/core
Orderable:　1,2 Chips
Cache L1:　32 KB I + 48 KB D on chip per core
　L2:　　1.25 MB I+D on chip per core
　L3:　　42 MB I+D on chip per chip
　Other:　None
Memory:　256 GB (16 x 16 GB 1Rx4 PC4-3200AA-R)
Storage:　1 x 480 GB SATA SSD
Other:　None

Software

OS:　CentOS Linux release 8.4.2105
　　Kernel 4.18.0-305.3.1.el8.x86_64
Compiler:　C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
　　Compiler Build 20201113 for Linux;
　　Fortran: Version 2021.1 of Intel Fortran Compiler
　　Classic Build 20201112 for Linux;
　　C/C++: Version 2021.1 of Intel C/C++ Compiler
　　Classic Build 20201112 for Linux
Parallel:　Yes
Firmware:　Version 1.1a released Jun-2021
File System:　xfs
System State:　Run level 3 (multi-user)
Base Pointers:　64-bit
Peak Pointers:　64-bit
Other:　jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of
　　additional power usage.

　　　Standard Performance Evaluation Corporation (info@spec.org)　　　https://www.spec.org/

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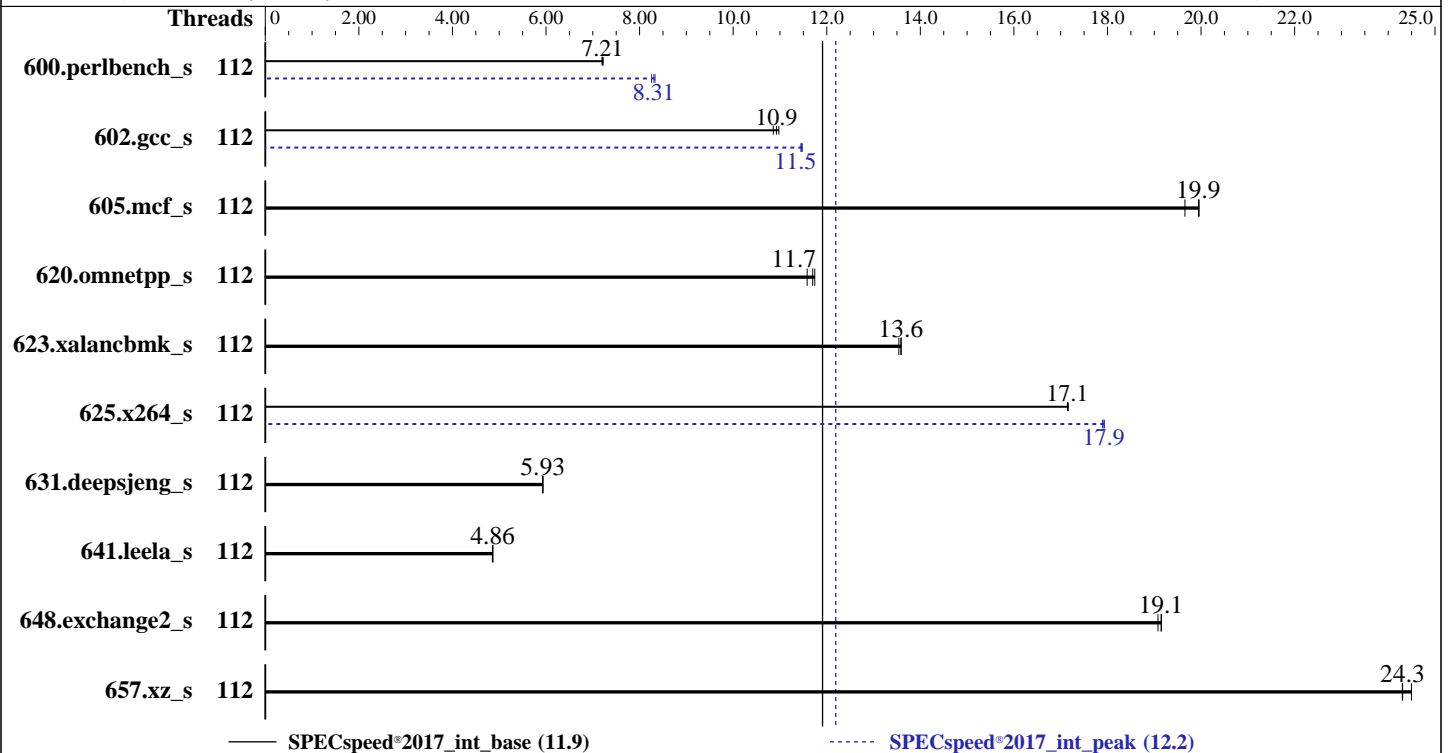SPECspeed®2017_int_peak = 12.2

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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	112	247	7.20	**246**	**7.21**	246	7.22	112	**214**	**8.31**	215	8.26	213	8.33
602.gcc_s	112	367	10.9	363	11.0	**364**	**10.9**	112	348	11.4	**348**	**11.5**	347	11.5
605.mcf_s	112	**237**	**19.9**	240	19.7	237	20.0	112	**237**	**19.9**	240	19.7	237	20.0
620.omnetpp_s	112	**139**	**11.7**	139	11.7	141	11.6	112	**139**	**11.7**	139	11.7	141	11.6
623.xalancbmk_s	112	104	13.6	**104**	**13.6**	105	13.5	112	104	13.6	**104**	**13.6**	105	13.5
625.x264_s	112	103	17.2	103	17.1	**103**	**17.1**	112	**98.4**	**17.9**	98.4	17.9	98.6	17.9
631.deepsjeng_s	112	**242**	**5.93**	242	5.93	242	5.93	112	**242**	**5.93**	242	5.93	242	5.93
641.leela_s	112	**351**	**4.86**	351	4.85	351	4.86	112	**351**	**4.86**	351	4.85	351	4.86
648.exchange2_s	112	154	19.1	153	19.2	**154**	**19.1**	112	154	19.1	153	19.2	**154**	**19.1**
657.xz_s	112	**254**	**24.3**	252	24.5	254	24.3	112	**254**	**24.3**	252	24.5	254	24.3
SPECspeed®2017_int_base =		**11.9**												
SPECspeed®2017_int_peak =									**12.2**					

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"
```

General Notes

```
Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>       /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

```
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
```

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Hardware Availability: Apr-2021
Software Availability: Jun-2021

General Notes (Continued)

sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Platform Notes

```
BIOS Settings:
Power Technology set to Custom
Power Performance Tuning set to BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode set to Performance
LLC Dead Line Alloc set to Disable

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on localhost.localdomain Sat Jul 31 05:36:30 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
       2  "physical id"s (chips)
       112 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 28
       siblings  : 56
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27

 From lscpu from util-linux 2.32.1:
       Architecture:        x86_64
       CPU op-mode(s):      32-bit, 64-bit
       Byte Order:          Little Endian
       CPU(s):              112
       On-line CPU(s) list: 0-111
       Thread(s) per core:  2
       Core(s) per socket:  28
       Socket(s):           2
       NUMA node(s):        2
       Vendor ID:           GenuineIntel
       BIOS Vendor ID:      Intel(R) Corporation
       CPU family:          6
       Model:               106
       Model name:          Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
```

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CPU2017 License: 006042	**Test Date:**	Jul-2021
Test Sponsor: Netweb Pte Ltd	**Hardware Availability:** Apr-2021
Tested by: Tyrone Systems	**Software Availability:** Jun-2021

Platform Notes (Continued)

```
        BIOS Model name:      Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
        Stepping:             6
        CPU MHz:              3400.442
        CPU max MHz:          3500.0000
        CPU min MHz:          800.0000
        BogoMIPS:             5200.00
        Virtualization:       VT-x
        L1d cache:            48K
        L1i cache:            32K
        L2 cache:             1280K
        L3 cache:             43008K
        NUMA node0 CPU(s):    0-27,56-83
        NUMA node1 CPU(s):    28-55,84-111
        Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
    aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
    xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
    avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single
    intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept
    vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a
    avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
    avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
    cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts avx512vbmi umip pku
    ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme
    avx512_vpopcntdq la57 rdpid fsrm md_clear pconfig flush_l1d arch_capabilities

  /proc/cpuinfo cache data
     cache size : 43008 KB

  From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
    56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83
    node 0 size: 128601 MB
    node 0 free: 127727 MB
    node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
    53 54 55 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106
    107 108 109 110 111
    node 1 size: 128972 MB
    node 1 free: 128416 MB
    node distances:
    node   0   1
      0:  10  20
      1:  20  10
```

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Platform Notes (Continued)

```
From /proc/meminfo
   MemTotal:       263755836 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB


/sbin/tuned-adm active
    Current active profile: throughput-performance


/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
   performance


From /etc/*release* /etc/*version*
   centos-release: CentOS Linux release 8.4.2105
   centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
   os-release:
      NAME="CentOS Linux"
      VERSION="8"
      ID="centos"
      ID_LIKE="rhel fedora"
      VERSION_ID="8"
      PLATFORM_ID="platform:el8"
      PRETTY_NAME="CentOS Linux 8"
      ANSI_COLOR="0;31"
   redhat-release: CentOS Linux release 8.4.2105
   system-release: CentOS Linux release 8.4.2105
   system-release-cpe: cpe:/o:centos:centos:8

uname -a:
   Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC
   2021 x86_64 x86_64 x86_64 GNU/Linux


Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                     Not affected
CVE-2018-3620 (L1 Terminal Fault):                  Not affected
Microarchitectural Data Sampling:                   Not affected
CVE-2017-5754 (Meltdown):                           Not affected
CVE-2018-3639 (Speculative Store Bypass):           Mitigation: Speculative Store
                                                    Bypass disabled via prctl and
                                                    seccomp
CVE-2017-5753 (Spectre variant 1):                  Mitigation: usercopy/swapgs
                                                    barriers and __user pointer
                                                    sanitization
CVE-2017-5715 (Spectre variant 2):                  Mitigation: Enhanced IBRS, IBPB:
                                                    conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):            Not affected
```

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Platform Notes (Continued)

```
 run-level 3 Jul 31 05:30

 SPEC is set to: /home/cpu2017
    Filesystem          Type  Size  Used Avail Use% Mounted on
    /dev/mapper/cl-home xfs   163G   88G   75G  55% /home

 From /sys/devices/virtual/dmi/id
    Vendor:           Tyrone Systems
    Product:          Tyrone Camarero SDI100A2R-22
    Product Family: SMC X12
    Serial:           123456789

 Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
 interpret this section. The 'dmidecode' program reads system data which is "intended to
 allow hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
       16x Samsung M393A2K40DB3-CWE 16 GB 1 rank 3200

 BIOS:
    BIOS Vendor:        American Megatrends International, LLC.
    BIOS Version:       1.1a
    BIOS Date:          06/25/2021
    BIOS Revision:      5.22

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C        | 600.perlbench_s(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
         | 625.x264_s(base, peak) 657.xz_s(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

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Compiler Version Notes (Continued)

```
================================================================================
C        | 600.perlbench_s(peak)
--------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C        | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
         | 625.x264_s(base, peak) 657.xz_s(base, peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C++      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
         | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
Fortran | 648.exchange2_s(base, peak)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

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Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
```
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:
```
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc
```

Fortran benchmarks:
```
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries
```

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icx
```

600.perlbench_s: `icc`

C++ benchmarks:
```
icpx
```

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Peak Compiler Invocation (Continued)

Fortran benchmarks:
```
ifort
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

600.perlbench_s: `-Wl,-z,muldefs` `-prof-gen`(pass 1) `-prof-use`(pass 2)
`-xCORE-AVX512` `-ipo` `-O3` `-no-prec-div`
`-qopt-mem-layout-trans=4` `-fno-strict-overflow`
`-mbranches-within-32B-boundaries`
`-L/usr/local/je5.0.1-64/lib` `-ljemalloc`

602.gcc_s: `-m64` `-std=c11` `-Wl,-z,muldefs` `-fprofile-generate`(pass 1)
`-fprofile-use=default.profdata`(pass 2) `-xCORE-AVX512` `-flto`
`-Ofast`(pass 1) `-O3` `-ffast-math` `-qopt-mem-layout-trans=4`
`-mbranches-within-32B-boundaries`
`-L/usr/local/je5.0.1-64/lib` `-ljemalloc`

605.mcf_s: basepeak = yes

625.x264_s: `-DSPEC_OPENMP` `-fiopenmp` `-std=c11` `-m64` `-Wl,-z,muldefs`
`-xCORE-AVX512` `-flto` `-O3` `-ffast-math`
`-qopt-mem-layout-trans=4` `-fno-alias`
`-mbranches-within-32B-boundaries`
`-L/usr/local/je5.0.1-64/lib` `-ljemalloc`

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

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Peak Optimization Flags (Continued)

641.leela_s: `basepeak = yes`

Fortran benchmarks:

648.exchange2_s: `basepeak = yes`

The flags files that were used to format this result can be browsed at
`http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html`
`http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html`

You can also download the XML flags sources by saving the following links:
`http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml`
`http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml`

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-31 05:36:29-0400.
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