# SPEC CPU®2017 Integer Rate Result

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## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

$SPECrate^{®}2017\_int\_base = 275$

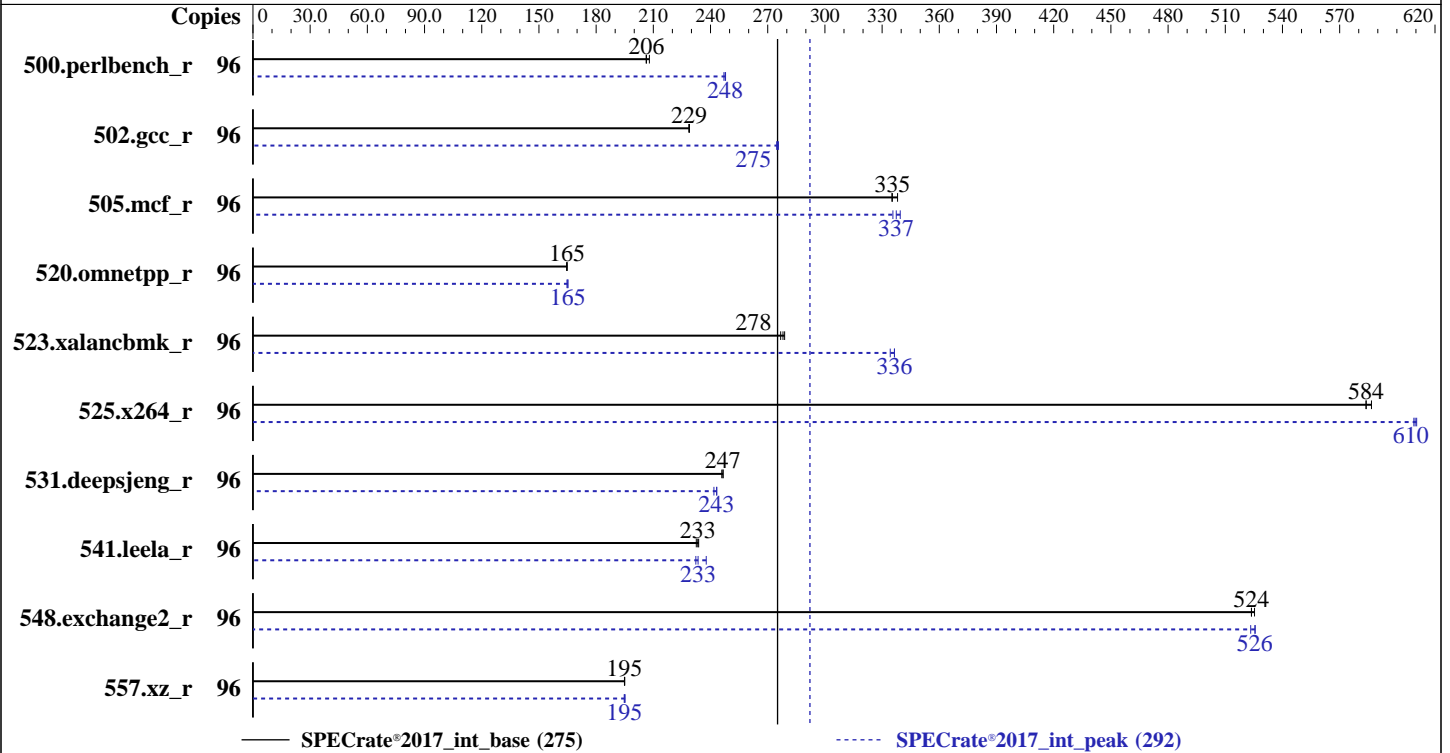$SPECrate^{®}2017\_int\_peak = 292$

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

| Copies | Benchmark | base | peak |
|---|---|---|---|
| 500.perlbench_r | 96 | 206 | 248 |
| 502.gcc_r | 96 | 229 | 275 |
| 505.mcf_r | 96 | 335 | 337 |
| 520.omnetpp_r | 96 | 165 | 165 |
| 523.xalancbmk_r | 96 | 278 | 336 |
| 525.x264_r | 96 | 584 | 610 |
| 531.deepsjeng_r | 96 | 247 | 243 |
| 541.leela_r | 96 | 233 | 233 |
| 548.exchange2_r | 96 | 524 | 526 |
| 557.xz_r | 96 | 195 | 195 |

—— SPECrate®2017_int_base (275)      ----- SPECrate®2017_int_peak (292)

## Hardware

CPU Name: Intel Xeon Gold 6126

 Max MHz: 3700

 Nominal: 2600

Enabled: 48 cores, 4 chips, 2 threads/core

Orderable: 2,4 Chips

Cache L1: 32 KB I + 32 KB D on chip per core

 L2: 1 MB I+D on chip per core

 L3: 19.25 MB I+D on chip per chip

 Other: None

Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)

Storage: 1 x 1 TB HDD, 7.2K RPM

Other: None

## Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default

Compiler: C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux

Parallel: No

Firmware: Version 3.1.3e released Jun-2018

File System: xfs

System State: Run level 3 (multi-user)

Base Pointers: 64-bit

Peak Pointers: 32/64-bit

Other: jemalloc memory allocator V5.0.1

Power Management: --

Standard Performance Evaluation Corporation (info@spec.org)

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| | |
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## Results Table

| Benchmark | Base | | | | | | Peak | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 500.perlbench_r | 96 | 741 | 206 | **740** | **206** | 735 | 208 | 96 | **617** | **248** | 617 | 248 | 619 | 247 |
| 502.gcc_r | 96 | 595 | 229 | **594** | **229** | 594 | 229 | 96 | 493 | 276 | 495 | 275 | **494** | **275** |
| 505.mcf_r | 96 | 459 | 338 | **463** | **335** | 463 | 335 | 96 | 462 | 336 | 457 | 340 | **460** | **337** |
| 520.omnetpp_r | 96 | 764 | 165 | **765** | **165** | 766 | 165 | 96 | **763** | **165** | 765 | 165 | 762 | 165 |
| 523.xalancbmk_r | 96 | 366 | 277 | **365** | **278** | 364 | 279 | 96 | **301** | **336** | 303 | 334 | 301 | 336 |
| 525.x264_r | 96 | 288 | 584 | **288** | **584** | 287 | 587 | 96 | 275 | 610 | **276** | **610** | 276 | 609 |
| 531.deepsjeng_r | 96 | 447 | 246 | **446** | **247** | 446 | 247 | 96 | **452** | **243** | 455 | 242 | 452 | 243 |
| 541.leela_r | 96 | 680 | 234 | **681** | **233** | 684 | 233 | 96 | **681** | **233** | 669 | 238 | 684 | 232 |
| 548.exchange2_r | 96 | 479 | 525 | **480** | **524** | 480 | 524 | 96 | **479** | **526** | 478 | 526 | 481 | 523 |
| 557.xz_r | 96 | 532 | 195 | 532 | 195 | **532** | **195** | 96 | **532** | **195** | 531 | 195 | 532 | 195 |
| **SPECrate®2017_int_base =** | | **275** | | | | | | | | | | | |
| **SPECrate®2017_int_peak =** | | **292** | | | | | | | | | | | |

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

 Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.5
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
 sync; echo 3>        /proc/sys/vm/drop_caches
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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## General Notes (Continued)

is mitigated in the system as tested and documented.

jemalloc: configured and built at default for
32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4,
and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or
https://github.com/jemalloc/jemalloc/releases

## Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-e8np Thu Jan 24 17:23:18 2019

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz
       4  "physical id"s (chips)
       96 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 12
       siblings  : 24
       physical 0: cores 0 1 3 5 6 8 9 10 11 12 13 14
       physical 1: cores 0 1 3 4 5 6 8 9 10 11 12 13
       physical 2: cores 0 2 3 4 5 8 9 10 11 12 13 14
       physical 3: cores 0 1 2 3 4 6 9 10 11 12 13 14

 From lscpu:
    Architecture:          x86_64
    CPU op-mode(s):        32-bit, 64-bit
    Byte Order:            Little Endian
    CPU(s):                96
    On-line CPU(s) list:   0-95
    Thread(s) per core:    2
```

**(Continued on next page)**

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### Platform Notes (Continued)

```
      Core(s) per socket:     12
      Socket(s):              4
      NUMA node(s):           8
      Vendor ID:              GenuineIntel
      CPU family:             6
      Model:                  85
      Model name:             Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz
      Stepping:               4
      CPU MHz:                1000.206
      CPU max MHz:            3700.0000
      CPU min MHz:            1000.0000
      BogoMIPS:               5194.44
      Virtualization:         VT-x
      L1d cache:              32K
      L1i cache:              32K
      L2 cache:               1024K
      L3 cache:               19712K
      NUMA node0 CPU(s):      0-2,5-7,48-50,53-55
      NUMA node1 CPU(s):      3,4,8-11,51,52,56-59
      NUMA node2 CPU(s):      12-14,18-20,60-62,66-68
      NUMA node3 CPU(s):      15-17,21-23,63-65,69-71
      NUMA node4 CPU(s):      24-26,29-31,72-74,77-79
      NUMA node5 CPU(s):      27,28,32-35,75,76,80-83
      NUMA node6 CPU(s):      36-39,42,43,84-87,90,91
      NUMA node7 CPU(s):      40,41,44-47,88,89,92-95
      Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
    xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
    dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
    retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
    avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
    clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
    cache size : 19712 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 8 nodes (0-7)
    node 0 cpus: 0 1 2 5 6 7 48 49 50 53 54 55
    node 0 size: 192095 MB
    node 0 free: 189646 MB
    node 1 cpus: 3 4 8 9 10 11 51 52 56 57 58 59
    node 1 size: 193528 MB
```

**(Continued on next page)**

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## Platform Notes (Continued)

```
   node 1 free: 191088 MB
   node 2 cpus: 12 13 14 18 19 20 60 61 62 66 67 68
   node 2 size: 193528 MB
   node 2 free: 191058 MB
   node 3 cpus: 15 16 17 21 22 23 63 64 65 69 70 71
   node 3 size: 193528 MB
   node 3 free: 191174 MB
   node 4 cpus: 24 25 26 29 30 31 72 73 74 77 78 79
   node 4 size: 193528 MB
   node 4 free: 191170 MB
   node 5 cpus: 27 28 32 33 34 35 75 76 80 81 82 83
   node 5 size: 193528 MB
   node 5 free: 191181 MB
   node 6 cpus: 36 37 38 39 42 43 84 85 86 87 90 91
   node 6 size: 193528 MB
   node 6 free: 191168 MB
   node 7 cpus: 40 41 44 45 46 47 88 89 92 93 94 95
   node 7 size: 193525 MB
   node 7 free: 191175 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  21  21
     1:  11  10  21  21  21  21  21  21
     2:  21  21  10  11  21  21  21  21
     3:  21  21  11  10  21  21  21  21
     4:  21  21  21  21  10  11  21  21
     5:  21  21  21  21  11  10  21  21
     6:  21  21  21  21  21  21  10  11
     7:  21  21  21  21  21  21  11  10

 From /proc/meminfo
    MemTotal:       1583914664 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 2
       # This file is deprecated and will be removed in a future service pack or release.
       # Please check /etc/os-release for details about this release.
    os-release:
       NAME="SLES"
       VERSION="12-SP2"
       VERSION_ID="12.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
```

**(Continued on next page)**

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## Platform Notes (Continued)

```
      ID="sles"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-e8np 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Jan 24 01:43

 SPEC is set to: /home/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sda1       xfs   894G  120G  774G  14% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
   Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

 (End of data from sysinfo program)
```

## Compiler Version Notes

```
==============================================================================
C        | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
  19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
         | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 502.gcc_r(peak)
------------------------------------------------------------------------------
```

**(Continued on next page)**

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```
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------------------------------------------------------------------------------


==============================================================================
C        | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
         | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++      | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
  19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
         | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++      | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
  19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
         | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

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## Compiler Version Notes (Continued)

```
==============================================================================
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

## Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

Fortran benchmarks:
`ifort -m64`

## Base Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-DSPEC_LP64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

## Base Optimization Flags

C benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`

C++ benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`

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# Base Optimization Flags (Continued)

C++ benchmarks (continued):
```
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

# Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.0.117/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):
```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.0.117/linux/compiler/lib/ia32_lin
```

Fortran benchmarks:
```
ifort -m64
```

# Peak Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

# Peak Optimization Flags

C benchmarks:

**(Continued on next page)**

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# Peak Optimization Flags (Continued)

500.perlbench_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-fno-strict-overflow -L/usr/local/je5.0.1-64/lib`
`-ljemalloc`

502.gcc_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-L/usr/local/je5.0.1-32/lib -ljemalloc`

505.mcf_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib`
`-ljemalloc`

525.x264_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -fno-alias`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

557.xz_r: `Same as 505.mcf_r`

C++ benchmarks:

520.omnetpp_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

523.xalancbmk_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: `Same as 520.omnetpp_r`

541.leela_r: `Same as 520.omnetpp_r`

Fortran benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.2019-01-15.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.2019-01-15.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

# SPEC CPU®2017 Integer Rate Result

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## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECrate®2017_int_base = 275

SPECrate®2017_int_peak = 292

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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