



SPEC® CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint®2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

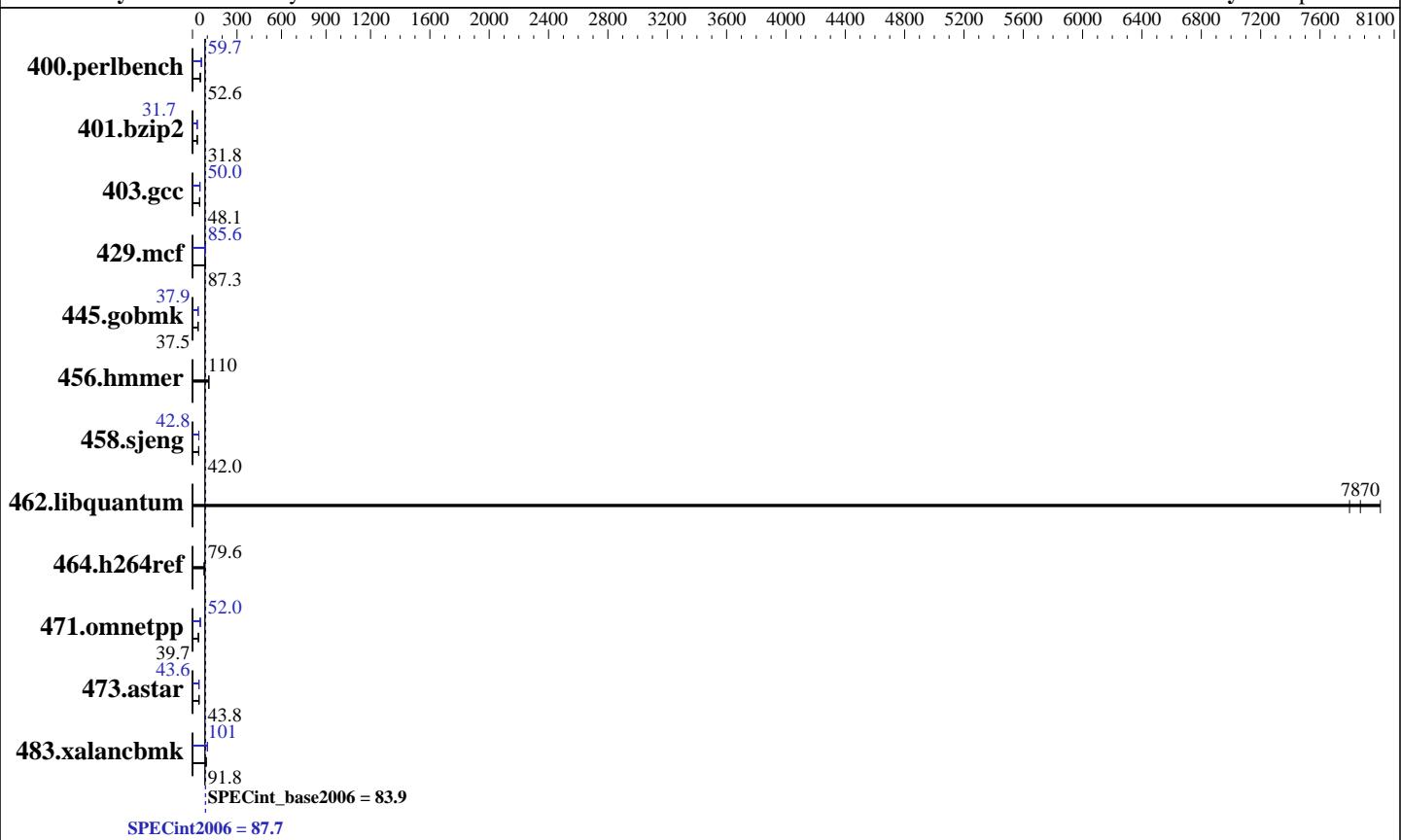
Test date: Nov-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Sep-2017



Hardware		Software	
CPU Name:	Intel Xeon Gold 6146	Operating System:	Red Hat Enterprise Linux Server release 7.3 (Maipo)
CPU Characteristics:	Intel Turbo Boost Technology up to 4.20 GHz	Compiler:	3.10.0-514.el7.x86_64
CPU MHz:	3200	Auto Parallel:	C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
FPU:	Integrated	File System:	xfs
CPU(s) enabled:	48 cores, 4 chips, 12 cores/chip	System State:	Run level 3 (multi-user)
CPU(s) orderable:	2,4 chips	Base Pointers:	32/64-bit
Primary Cache:	32 KB I + 32 KB D on chip per core	Peak Pointers:	32/64-bit
Secondary Cache:	1 MB I+D on chip per core	Other Software:	Microquill SmartHeap V10.2
L3 Cache:	24.75 MB I+D on chip per chip		
Other Cache:	None		
Memory:	768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)		
Disk Subsystem:	1 x 600 GB SAS HDD, 10K RPM		
Other Hardware:	None		



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

Test date: Nov-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Sep-2017

Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	186	52.6	186	52.6	186	52.6	164	59.7	164	59.6	164	59.7
401.bzip2	303	31.8	303	31.8	304	31.8	304	31.7	304	31.7	304	31.7
403.gcc	167	48.2	167	48.1	167	48.1	161	50.0	161	50.0	161	50.0
429.mcf	104	87.3	104	87.3	107	85.5	106	85.6	106	86.3	108	84.4
445.gobmk	280	37.5	279	37.5	279	37.6	277	37.9	277	37.9	277	37.9
456.hmmer	84.9	110	84.7	110	85.0	110	84.9	110	84.7	110	85.0	110
458.sjeng	288	42.0	288	42.0	288	42.0	283	42.7	283	42.8	283	42.8
462.libquantum	2.63	7870	2.66	7800	2.59	8010	2.63	7870	2.66	7800	2.59	8010
464.h264ref	281	78.9	278	79.7	278	79.6	281	78.9	278	79.7	278	79.6
471.omnetpp	158	39.6	157	39.7	155	40.3	121	51.5	117	53.2	120	52.0
473.astar	161	43.7	160	43.8	159	44.1	161	43.5	161	43.6	161	43.6
483.xalancbmk	75.2	91.8	75.0	92.0	75.5	91.4	68.3	101	68.3	101	68.7	100

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Disabled

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993

Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)

running on localhost.localdomain Wed Nov 22 01:02:41 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz

4 "physical id"s (chips)

48 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

Test date: Nov-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Sep-2017

Platform Notes (Continued)

following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 12
siblings   : 12
physical 0: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 1: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 2: cores 0 1 3 9 10 16 18 19 24 25 26 27
physical 3: cores 0 1 3 9 10 16 18 19 24 25 26 27
cache size : 25344 KB
```

```
From /proc/meminfo
MemTotal:      791031796 kB
HugePages_Total:      0
Hugepagesize:     2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
  NAME="Red Hat Enterprise Linux Server"
  VERSION="7.3 (Maipo)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="7.3"
  PRETTY_NAME="Red Hat Enterprise Linux Server 7.3 (Maipo)"
  ANSI_COLOR="0;31"
  CPE_NAME="cpe:/o:redhat:enterprise_linux:7.3:GA:server"
redhat-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)
system-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)
system-release-cpe: cpe:/o:redhat:enterprise_linux:7.3:ga:server
```

```
uname -a:
Linux localhost.localdomain 3.10.0-514.el7.x86_64 #1 SMP Wed Oct 19 11:24:13
EDT 2016 x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Jan 5 16:35

```
SPEC is set to: /home/cpu2006-1.2
Filesystem           Type  Size  Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs   225G   15G  211G   7% /home
Additional information from dmidecode:
```

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017Cisco Systems,
Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
Memory:
 96x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz
```

(End of data from sysinfo program)

The correct amount of Memory installed is 768 GB (48 x 16 GB)

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

Test date: Nov-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Sep-2017

Platform Notes (Continued)

and the dmidecode is reporting invalid number of DIMMs installed

Installed Memory:

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

General Notes

Environment variables set by runspec before the start of the run:

KMP_AFFINITY = "granularity=fine,compact"

LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

OMP_NUM_THREADS = "48"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/transparent_hugepage/enabled

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on
past performance using the historical hardware and/or
software described on this result page.

The system as described on this result page was formerly
generally available. At the time of this publication, it may
not be shipping, and/or may not be supported, and/or may fail
to meet other tests of General Availability described in the
SPEC OSG Policy document, <http://www.spec.org/osg/policy.html>

This measured result may not be representative of the result
that would be measured were this benchmark run with hardware
and software available as of the publication date.

Base Compiler Invocation

C benchmarks:

icc -m64

C++ benchmarks:

icpc -m64



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Nov-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Base Portability Flags

```
400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64  
401.bzip2: -DSPEC_CPU_LP64  
403.gcc: -DSPEC_CPU_LP64  
429.mcf: -DSPEC_CPU_LP64  
445.gobmk: -DSPEC_CPU_LP64  
456.hammer: -DSPEC_CPU_LP64  
458.sjeng: -DSPEC_CPU_LP64  
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX  
464.h264ref: -DSPEC_CPU_LP64  
471.omnetpp: -DSPEC_CPU_LP64  
473.astar: -DSPEC_CPU_LP64  
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch  
-auto-p32
```

C++ benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32  
-Wl,-z,muldefs -L/sh10.2 -lsmartheap64
```

Base Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64
```

```
400.perlbench: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

```
445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

C++ benchmarks (except as noted below):

```
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

```
473.astar: icpc -m64
```



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

Test date: Nov-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Sep-2017

Peak Portability Flags

```

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
 401.bzip2: -DSPEC_CPU_LP64
  403.gcc: -DSPEC_CPU_LP64
  429.mcf: -DSPEC_CPU_LP64
 445.gobmk: -D_FILE_OFFSET_BITS=64
 456.hammer: -DSPEC_CPU_LP64
  458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
 464.h264ref: -DSPEC_CPU_LP64
 471.omnetpp: -D_FILE_OFFSET_BITS=64
  473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

```

Peak Optimization Flags

C benchmarks:

```

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -qopt-prefetch

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div -auto-ilp32 -qopt-prefetch

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
          -qopt-malloc-options=3 -auto-ilp32

429.mcf: -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
          -qopt-prefetch -auto-p32

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2)

456.hammer: basepeak = yes

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -unroll4

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

```

C++ benchmarks:

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146,
3.20 GHz)

SPECint2006 = 87.7

SPECint_base2006 = 83.9

CPU2006 license: 9019

Test date: Nov-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Sep-2017

Peak Optimization Flags (Continued)

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-ra-region-strategy=block
-Wl,-z,muldefs -L/sh10.2 -lsmartheap

473.astar: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-auto-p32 -Wl,-z,muldefs -L/sh10.2 -lsmartheap64

483.xalancbmk: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-Wl,-z,muldefs -L/sh10.2 -lsmartheap

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Mon Feb 26 10:21:40 2018 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 23 February 2018.