SPEC® CINT2006 Result

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

SPECint®2006 =   40.2

SPECint_base2006 =   38.2

CPU2006 license: 9019
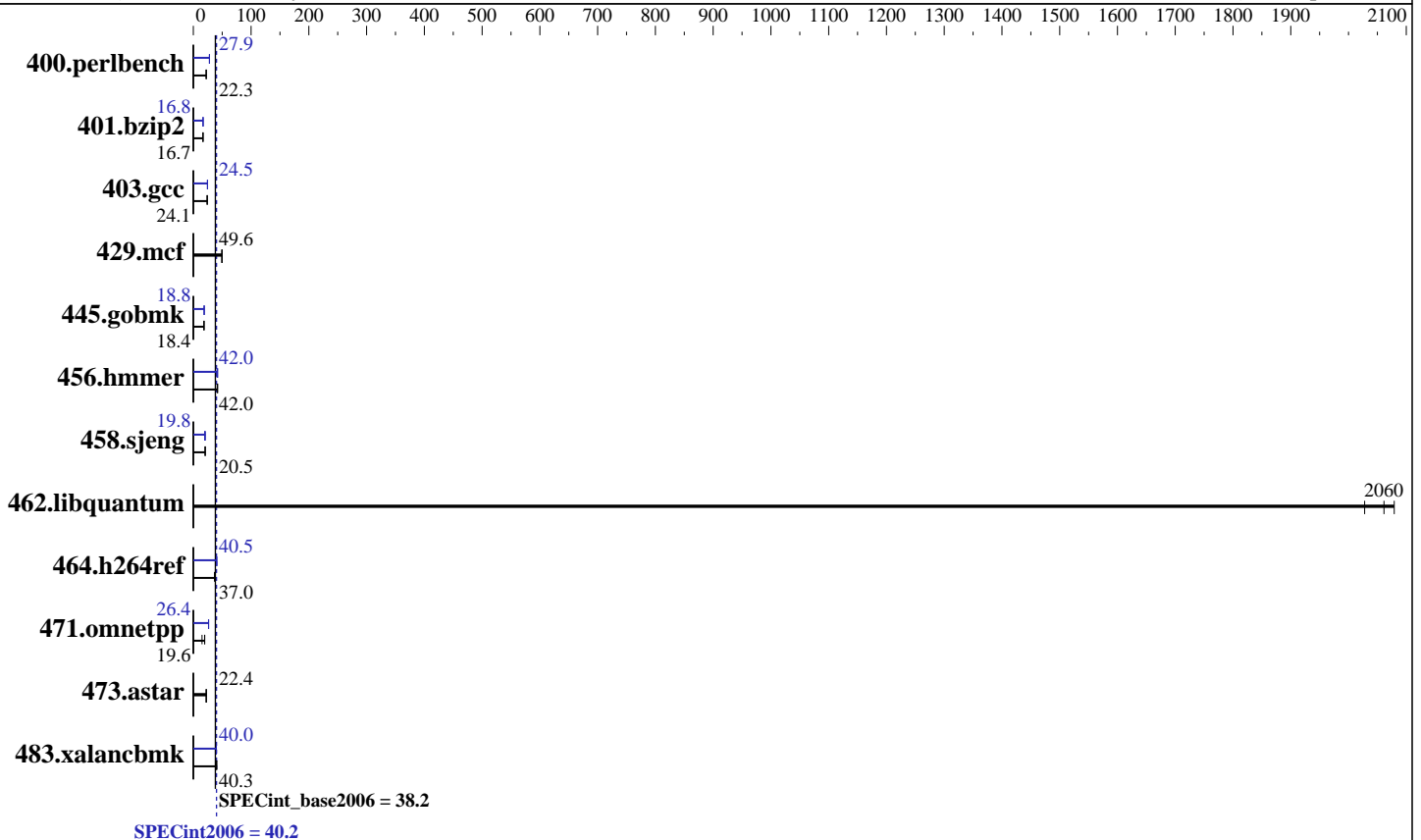
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2013

Hardware Availability: Dec-2013

Software Availability: Sep-2013

Graph scale: 0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100

Benchmark	Peak	Base
400.perlbench	27.9	22.3
401.bzip2	16.8	16.7
403.gcc	24.5	24.1
429.mcf		49.6
445.gobmk	18.8	18.4
456.hmmer	42.0	42.0
458.sjeng	19.8	20.5
462.libquantum		2060
464.h264ref	40.5	37.0
471.omnetpp	26.4	19.6
473.astar		22.4
483.xalancbmk	40.0	40.3

SPECint_base2006 = 38.2

SPECint2006 = 40.2

Hardware

CPU Name:	Intel Xeon E5-2620 v2
CPU Characteristics:	Intel Turbo Boost Technology up to 2.60 GHz
CPU MHz:	2100
FPU:	Integrated
CPU(s) enabled:	12 cores, 2 chips, 6 cores/chip
CPU(s) orderable:	1,2 chip
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core
L3 Cache:	15 MB I+D on chip per chip
Other Cache:	None
Memory:	256 GB (16 x 16 GB 2Rx4 PC3-14900R-13, ECC, running at 1600 MHz and CL7)
Disk Subsystem:	1 X 300 GB 15000 RPM SAS
Other Hardware:	None

Software

Operating System:	Red Hat Enterprise Linux Server release 6.4 (Santiago) 2.6.32-358.el6.x86_64
Compiler:	C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel:	Yes
File System:	ext4
System State:	Run level 3 (multi-user)
Base Pointers:	32/64-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V10.0

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Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	**437**	**22.3**	437	22.3	438	22.3	350	27.9	350	27.9	**350**	**27.9**
401.bzip2	578	16.7	577	16.7	**578**	**16.7**	573	16.8	573	16.8	**573**	**16.8**
403.gcc	334	24.1	**335**	**24.1**	335	24.0	329	24.5	328	24.5	**328**	**24.5**
429.mcf	183	49.9	185	49.3	**184**	**49.6**	183	49.9	185	49.3	**184**	**49.6**
445.gobmk	569	18.4	569	18.4	**569**	**18.4**	558	18.8	**558**	**18.8**	558	18.8
456.hmmer	**222**	**42.0**	226	41.3	222	42.0	222	42.0	228	40.9	**222**	**42.0**
458.sjeng	**590**	**20.5**	590	20.5	590	20.5	580	20.9	**612**	**19.8**	612	19.8
462.libquantum	**10.1**	**2060**	9.97	2080	10.2	2030	**10.1**	**2060**	9.97	2080	10.2	2030
464.h264ref	599	37.0	598	37.0	**599**	**37.0**	547	40.4	**547**	**40.5**	547	40.5
471.omnetpp	**318**	**19.6**	415	15.1	318	19.7	238	26.3	235	26.6	**237**	**26.4**
473.astar	313	22.4	**313**	**22.4**	313	22.4	313	22.4	**313**	**22.4**	313	22.4
483.xalancbmk	170	40.6	173	39.8	**171**	**40.3**	**173**	**40.0**	173	40.0	173	39.9

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Platform Notes

```
   BIOS Settings:
   Intel HT Technology = Disabled
   CPU performance set to HPC
   Power Technology set to Custom
   CPU Power State C6 set to Enabled
   CPU Power State C1 Enhanced set to Disabled
   Energy Performance policy set to Performance
   Memory RAS configuration set to Maximum Performance
   DRAM Clock Throttling Set to Performance
   LV DDR Mode set to Performance-mode
   DRAM Refresh Rate Set to 1x
    Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
    $Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
    running on B200M3-IVB Sat Dec  7 05:21:12 2013

    This section contains SUT (System Under Test) info as seen by
    some common utilities.  To remove or add to this section, see:
      http://www.spec.org/cpu2006/Docs/config.html#sysinfo

    From /proc/cpuinfo
       model name : Intel(R) Xeon(R) CPU E5-2620 v2 @ 2.10GHz
          2 "physical id"s (chips)
          12 "processors"
```

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Platform Notes (Continued)

```
   cores, siblings (Caution: counting these is hw and system dependent.  The
   following excerpts from /proc/cpuinfo might not be reliable.  Use with
   caution.)
      cpu cores : 6
      siblings  : 6
      physical 0: cores 0 1 2 3 4 5
      physical 1: cores 0 1 2 3 4 5
   cache size : 15360 KB

 From /proc/meminfo
    MemTotal:      264464248 kB
    HugePages_Total:        0
    Hugepagesize:       2048 kB

 /usr/bin/lsb_release -d
    Red Hat Enterprise Linux Server release 6.4 (Santiago)

 From /etc/*release* /etc/*version*
    redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
    system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
    system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

 uname -a:
    Linux B200M3-IVB 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Dec 7 05:20

 SPEC is set to: /opt/cpu2006-1.2
    Filesystem    Type    Size  Used Avail Use% Mounted on
    /dev/sda1     ext4    275G   39G  222G  15% /

 Additional information from dmidecode:
   BIOS Cisco Systems, Inc. B200M3.2.1.3a.0.082320131800 08/23/2013
   Memory:
    16x 0xAD00 HMT42GR7AFR4C-RD 16 GB 1600 MHz 2 rank
    8x NO DIMM NO DIMM

 (End of data from sysinfo program)
```

General Notes

```
 Environment variables set by runspec before the start of the run:
 LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"
 OMP_NUM_THREADS = "12"

  Binaries compiled on a system with 1x Core i7-860 CPU + 8GB
  memory using RedHat EL 6.4
  Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
  runspec command invoked through numactl i.e.:
```

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General Notes (Continued)

```
numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
```
icc -m64
```

C++ benchmarks:
```
icpc -m64
```

Base Portability Flags

```
400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
  401.bzip2: -DSPEC_CPU_LP64
    403.gcc: -DSPEC_CPU_LP64
    429.mcf: -DSPEC_CPU_LP64
  445.gobmk: -DSPEC_CPU_LP64
  456.hmmer: -DSPEC_CPU_LP64
   458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
 464.h264ref: -DSPEC_CPU_LP64
 471.omnetpp: -DSPEC_CPU_LP64
   473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:
```
-xSSE4.2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32
```

C++ benchmarks:
```
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh -lsmartheap64
```

Base Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

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Peak Compiler Invocation

C benchmarks (except as noted below):
    `icc -m64`

    400.perlbench: `icc -m32`

      445.gobmk: `icc -m32`

    464.h264ref: `icc -m32`

C++ benchmarks (except as noted below):
    `icpc -m32`

      473.astar: `icpc -m64`

Peak Portability Flags

    400.perlbench: `-DSPEC_CPU_LINUX_IA32`
        401.bzip2: `-DSPEC_CPU_LP64`
         403.gcc: `-DSPEC_CPU_LP64`
         429.mcf: `-DSPEC_CPU_LP64`
      456.hmmer: `-DSPEC_CPU_LP64`
       458.sjeng: `-DSPEC_CPU_LP64`
    462.libquantum: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX`
        473.astar: `-DSPEC_CPU_LP64`
    483.xalancbmk: `-DSPEC_CPU_LINUX`

Peak Optimization Flags

C benchmarks:

    400.perlbench: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)`
               `-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)`
               `-opt-prefetch -ansi-alias`

      401.bzip2: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)`
               `-O3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32`
               `-opt-prefetch -ansi-alias`

        403.gcc: `-xSSE4.2 -ipo -O3 -no-prec-div -inline-calloc`
               `-opt-malloc-options=3 -auto-ilp32`

        429.mcf: `basepeak = yes`

      445.gobmk: `-xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)`
               `-ansi-alias`

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Peak Optimization Flags (Continued)

456.hmmer: `-xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32 -ansi-alias`

458.sjeng: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4`

462.libquantum: `basepeak = yes`

464.h264ref: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll2 -ansi-alias`

C++ benchmarks:

471.omnetpp: `-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-ra-region-strategy=block         -ansi-alias -Wl,-z,muldefs -L/sh -lsmartheap`

473.astar: `basepeak = yes`

483.xalancbmk: `-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -ansi-alias -Wl,-z,muldefs -L/sh -lsmartheap`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

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Tested with SPEC CPU2006 v1.2.
Report generated on Thu Jul 24 20:15:32 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 8 January 2014.